Viola

Cell Library Characterization, Validation and Variation Modeling

SILVACO

Overview

Viola™ is a unique, all-inclusive package for fast and accurate characterization of digital cell libraries including I/Os. The package includes Silvaco SmartSpiceTM with fully automated stimulus generation, a library model checker, and a databook generator.

The characterization engine performs detailed cell circuit analysis that automatically determines the required set of stimuli and creates SPICE decks to perform all characterization measurements for both combinational and sequential digital logic cells.

Library quality management ensures characterized libraries are qualified and evaluated against a series of test circuits to ensure SPICE-level accuracy and correlation with static timing analysis.

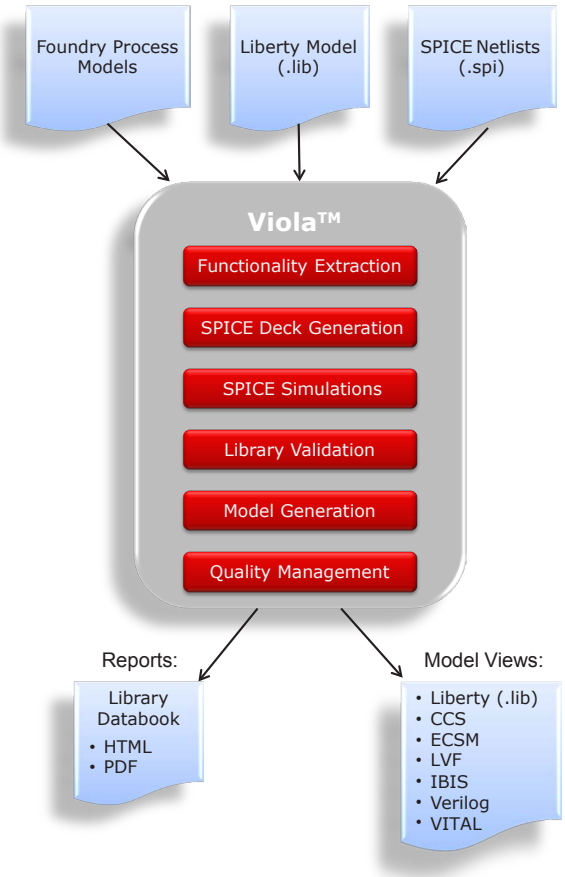
Key Features and Benefits

- Tight integration with SmartSpice simulator and the Silvaco tool flow
- Full integration with HSPICE® and Spectre® simulators
- Advanced characterization for timing, power and noise through current source modeling (CCS and ECSM), ensures characterization accuracy
- Supports variation-aware timing models for advanced process nodes in Liberty Variation Format (LVF), with performance optimizations
- Automatic logic recognition from the SPICE netlist of digital cells
- Fully automated SPICE deck generation, based on both cell parameters and functionality, ensures all necessary logical combinations are covered
- Customization of stimuli and measurements to support characterization of complex, non-standard cells
- Automatic determination of lookup table ranges and indices based on user-defined constraints
- Full integration with the databook generator in Silvaco Liberty AnalyzerTM provides hierarchical databooks for easy navigation with a HTML browser
- Silvaco Design Audit™ qualifies the accuracy and completeness of the generated views
- Powerful Tcl and Perl scripting environments

Library Quality Management™

With the Library Quality Management option, characterized libraries are qualified and evaluated against a series of test circuits to ensure that results obtained are accurate and consistent all the way through static timing analysis (STA) and sign-off. Viola generates a comparison report that will highlight any discrepancies that may require further calibration and characterization. This functionality is essential when:

- Foundries provide updated transistor models
- Introducing new tools or versions of tools into the flow (e.g. new SPICE version, STA tool, etc.)
- Qualifying or evaluating different timing models (e.g. NLDM vs. CCS or ECSM)
- Running at additional PVT corners where standard cells can become significantly nonlinear in their behavior



Completeness

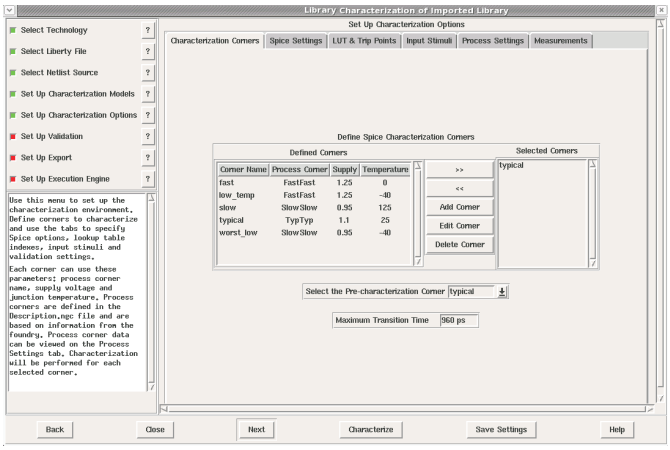
- Supports fully configurable two-dimensional and three-dimensional lookup tables for non-linear delay model characterization (NLDM) and Current Source Model characterization (both CCS and ECSM)
- Accurate input waveform generation from pre-cell drivers and multi-point PWL waveforms
- Scalable parallel execution of SPICE simulations through:
  – LSF™ from Platform Computing®
  – SUN® Grid Engine (SGE)
  – Multi-threaded processing
- Intuitive wizard interface for commonly used settings as well as extensive advanced configuration options for additional characterization parameters
- Built-in verification of stimuli, results, and model
- Unique constraint validation to verify if Liberty constraint values match input settings
- Consistency check through corners and models
- Re-characterization of any existing Liberty file
- Flexible databook generator providing HTML and PDF output
- Full Perl and Tcl scripting interface support

Cell Types

- Single and multi-output combinational cells including differential cells and tri-state outputs
- Sequential and combinational one-hot cells
- Sequential and combinational multibit cells
- Complex latches and flip-flops including SR-latches and flip-flops
- Low power cells such as always-on, level shifters, power switches, and retention flip-flops
- I/O pads with multiple voltage supplies and contention conditions
- Custom cells

Measurements

- State-dependent propagation delay and output transition time
- Minimum pulse width
- Setup, hold, recovery, and removal
- State-dependent internal static, dynamic, switching, leakage, and average power
- Input pin capacitance
- CCS and ECSM timing, power, and noise
- Zero cycle checks



Viola characterization setup wizard.

Inputs

- Liberty™ library model file, including PG-pin syntax
- Extracted cell netlists
- Foundry provided transistor models

Outputs

- Liberty (.lib) formatted library, with CCS and ECSM timing, power, and noise
- Liberty (.lib) including LVF for Variation-Aware libraries
- IBIS models for I/O
- Verilog and VITAL views
- Library databook in HTML and PDF format

Platform Support

- Red Hat Enterprise Linux® version 6 (x86 or x86-64)
- Red Hat Enterprise Linux® version 7

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