Victory Process

3D Process Simulator

SILVACO

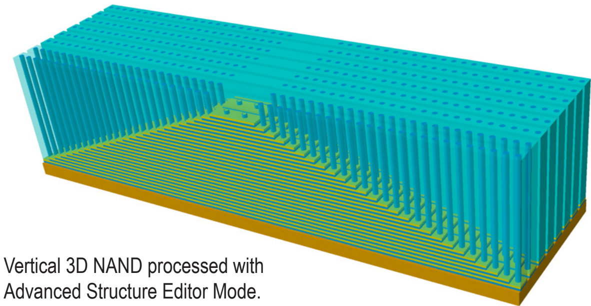
Victory Process is a general purpose layout driven 1D, 2D and 3D process and stress simulator including etching, deposition, implantation, diffusion, oxidation and stress simulation capabilities.

Features

- Fast 3D structure prototyping capability enables the in-depth physical analysis of specific processing issues
- Supports double side wafer processing simulation
- Comprehensive simulation support for compound materials, including variable compositions
- Comprehensive set of diffusion models: Fermi, twodim, single-pair, and five-stream
- Comprehensive full flow stress analysis , including stress induced by lattice mismatch, thermal mismatch, deposition and physical oxidation
- Extremely accurate and fast Monte Carlo implant simulation
- Efficient multi-threading of time critical operations of implantation, diffusion, oxidation, and physical etching and deposition
- Multi-particle flux models for physical deposition and etching with substrate material redeposition
- Open architecture allows easy introduction and modification of customer specific physical models for etching, deposition and annealing
- Seamless link to 3D device simulators including structure mirroring, adaptive doping refinement and electrode specification
- Parametrized layout specification as part of the simulation flow
- Convenient mesh specification based on layout features as well as manual mesh adaptation within the simulation flow
- Easy to learn, powerful debug mode and user friendly SUPREM-like syntax (Athena compatibility)
- Convenient calibration platform and fast process testing with 2D mode (no need to run 3D for calibration)
- Automatic switching from 1D, 2D and 3D mode as well as structure mirroring during process simulation to optimize simulation time

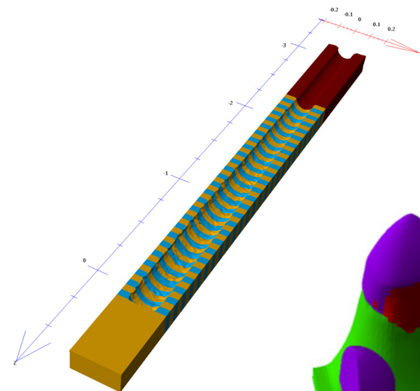
Victory Process has two modes of operation:

- The **Advanced structure editor** mode, also called cell mode, is for fast proto-typing of 3D structures, such as image sensors, SRAM cells or FinFETs, where structure output meshing algorithms are optimized for loading into 3D device simulators for subsequent electrical characterization.

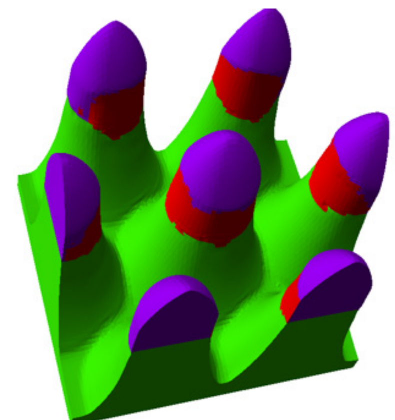


Vertical 3D NAND processed with Advanced Structure Editor Mode.

- **Process simulator mode**, is a full feature, level set based 1D, 2D and 3D process and stress simulator, more suited to process based analysis, such as complex ion beam milling experiments and stress dependent oxidation analysis etc.



Simulation of a gate etch in a 3D NAND with process simulator mode.



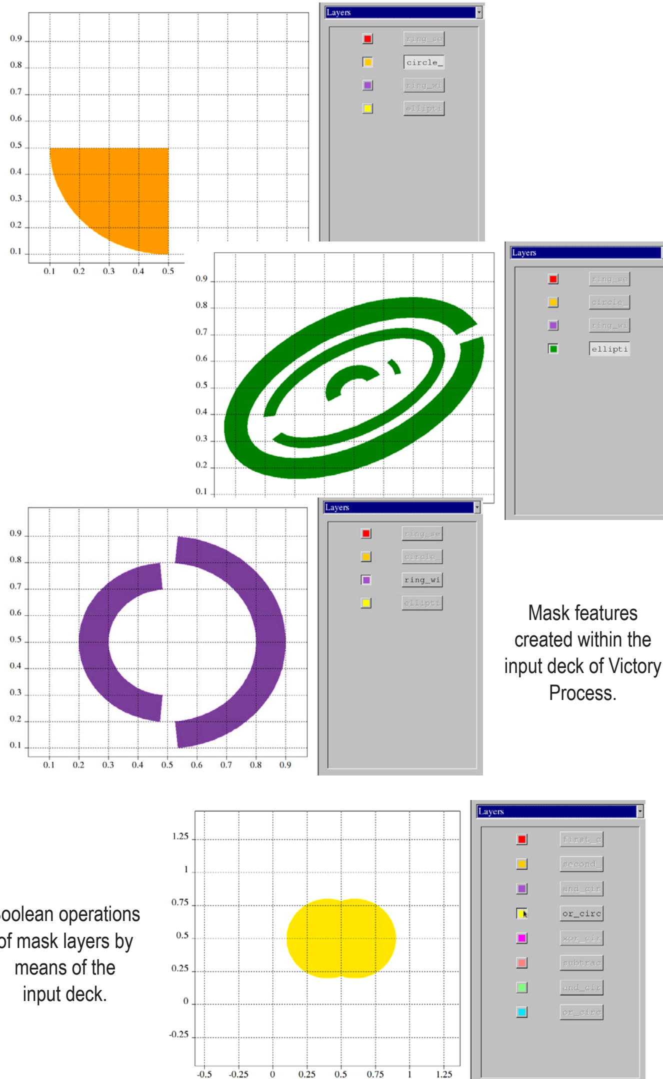
Formation of magnetic tunnel junction pillars simulated in process simulation mode.

This brochure first shows examples and features that are common to both modes of operation, such as implantation, diffusion, epitaxy and stress analysis and then describes features that are exclusive only to the advanced structure editor mode or to the advanced process simulator mode.

Features Common to Advanced Structure Editor and Process Simulator Modes

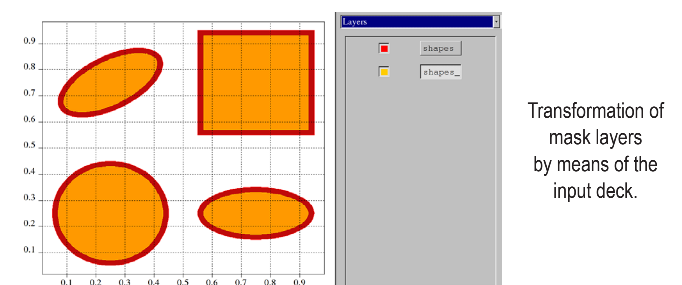
Comprehensive Layout Handling

- Specification of layouts within the simulation flow with a comprehensive set of primitives, enables complex parametrized layouts
- Handles predefined layouts in gds as well as SILVACO native mask format
- Allows modification of predefined layouts (shift, resize and boolean operations)
- Generates mask layers on the basis of LVS rule deck



Mask features created within the input deck of Victory Process.

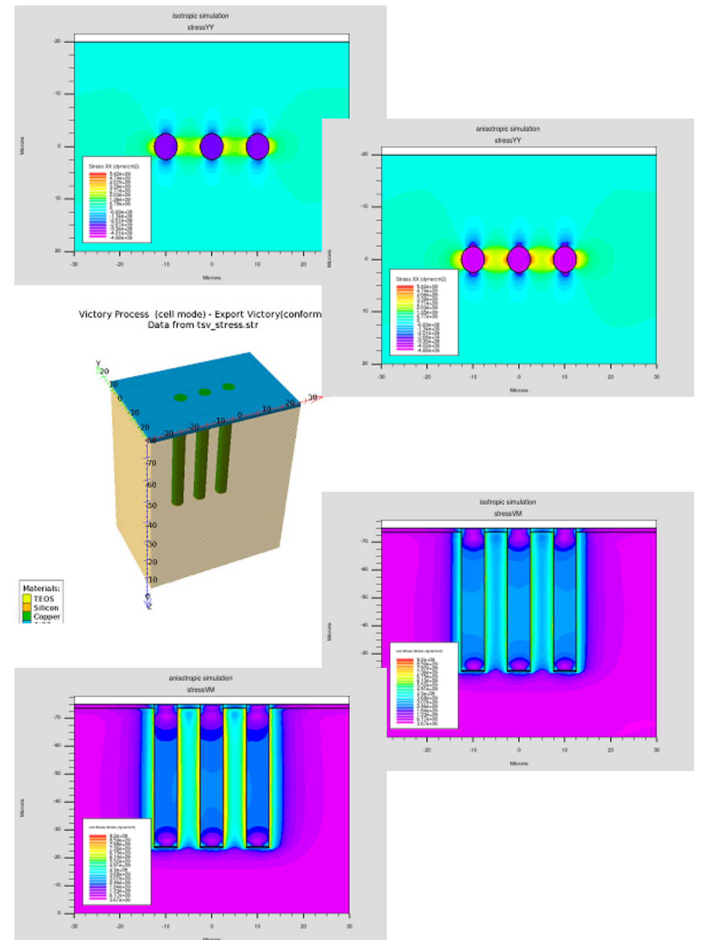
Boolean operations of mask layers by means of the input deck.



Transformation of mask layers by means of the input deck.

Stress History Simulation

- Simulation of the full stress history of all processing steps but also allows for single step stress analysis
- Accounts for multiple processing induced stress sources including deposition induced intrinsic stress, lattice mismatch stress, thermal mismatch stress and oxidation induced stress
- Accounts for stress feedback on oxidation
- Handles graded compound substrates as well as graded epitaxal compound layers



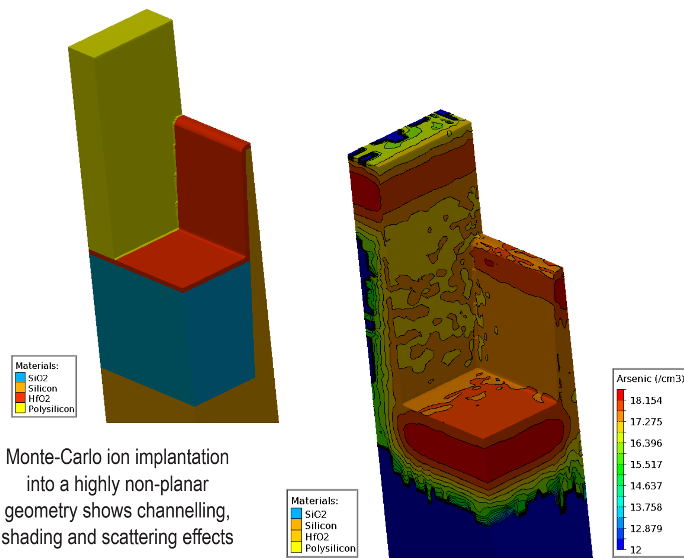
Geometry and stress profile in TSV structure when isotropic (middle) and an-isotropic (right) material properties are applied.

Analytical Ion Implantation

- Experimentally verified Pearson and dual Pearson implant models
- Extended implant moments tables with energy, dose, tilt, and rotation variations
- Support for user specific implantation profiles as well as moment tables
- Fully multi-threaded with run time reduction almost linearly proportional with number of CPUs

Monte Carlo Implantation

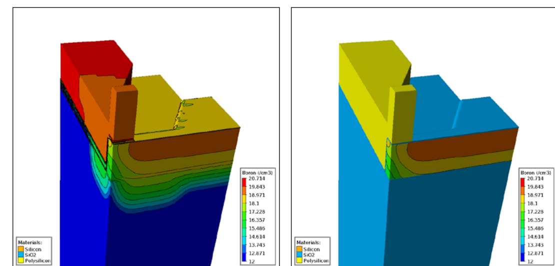
- Supports moments extraction on by Monte-Carlo implantation module
- Supports loading 3D profiles obtained by Monte-Carlo simulation
- Supports loading 1D experimental profiles
- Very accurate ion distributions in both crystalline and amorphous materials forming arbitrary geometries and multi-layer structures
- Supports user defined materials
- Material properties can be configured in the open material database
- Accurately calibrated for wide range of energies starting as low as 200 eV and spanning to the high MeV range
- Calibrated implantation into diamond and hexagonal type crystalline materials : Silicon, SiC, GaN
- Support arbitrary substrate orientation
- Accounts for all complex implantation effects such as reflections, re-implantation and shadowing even in deep trenches and voids
- Handles arbitrary implant directions
- Applies 3D binary collision approximation which predicts channeling not only into primary channel but in all possible secondary channels and crystallographic planes
- Provides time efficient and cost effective solutions for important technology issues such as shallow junction formation, multiple implants and pre-amorphization, HALO implants, retrograde well formation, and well proximity effect
- Fully multi-threaded with run time reduction almost linearly proportional with number of CPUs



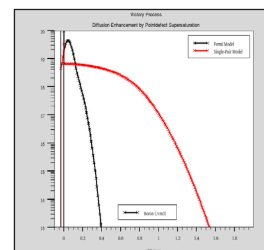
Monte-Carlo ion implantation into a highly non-planar geometry shows channelling, shading and scattering effects

Diffusion

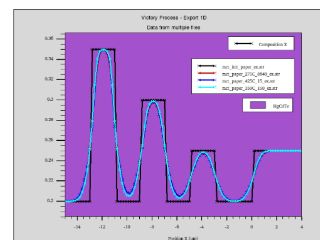
- Twodim, Fermi and grainbased diffusion model compatible with Athena/SSuprem4
- Simulation of multiple dopant diffusion
- Accounts for solid solubility, dopant activation, and segregation at material interfaces
- Continuity interface conditions for materials with sharp change in composition, like Silicon to SiGe or two regions of SiGe
- Fully multi-threaded equation assembler and linear solver provide substantial speed improvement on multi-core computers
- Simulation of transient enhanced diffusion effects
- Three-stream and five-stream diffusion models
- Point defect trapping and clustering models
- Impurity segregation at all material interfaces
- Impurity activation and solid solubility
- Diffusion in compound semiconductors like HgCdTe, InP, SiGe, SiGeC taking into account composition dependencies
- Simulation of the re-distribution of the material composition in compound semiconductors like HgCdTe
- Discontinous material interface model for heterostructure devices
- Simulation of oxidation mediated diffusion
- Simulation of flash annealing as well as laser annealing with user defined temperature profiles which can vary in time and space

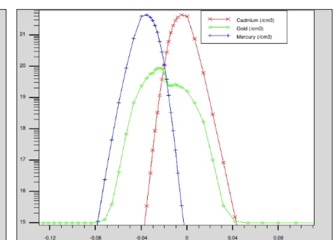


Boron distribution in a complex structure after analytical implant and Fermi diffusion.



Comparison of Fermi and 3-stream diffusion model in the presence of interstitial super-saturation.





Re-distribution of the HgCdTe composition due to annealing at various temperatures - Cadmium and Mercury as well as the dopants are diffusing simultaneously.

Diffusion

- Epitaxial growth of single atomic as well as compound material
- Accounts for doping re-distribution during epitaxy
- Handles graded composition during epitaxy
- Support for complex temperature profiles

Open Material Database

- Full access to all material and modeling data
- Supports user specific material databases and well as simulation specific material databases
- Definition of simulation specific materials by interitance
- Functional layer of the material database enables convenient modification as well as extension of material models
- Interface to open annealing model library for advanced material model development
- All Victory Products share one material database

Open Modeling Interface Capabilities

- Definition of model species
- Definition of model parameters
- Definition of reaction functions
- Configuration of the PDE system

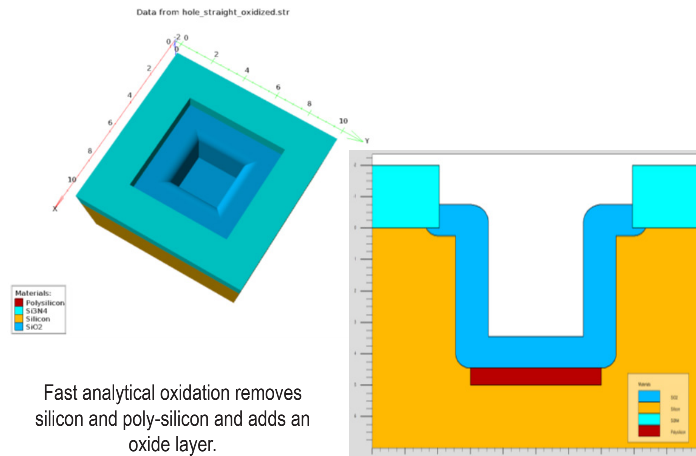
Device Meshing Interface

- Support for various mesh types
- Extensive refinement capabilities for all mesh types including global refinement, interface refinement, junction refinement, shape refinement
- Supports aspect ratio aligned an-isotropic meshing
- Structure modification by mirroring, cropping and slicing operations

Advanced Structure Editor Mode

Fast Geometrical Etching Deposition Empirical Oxidation

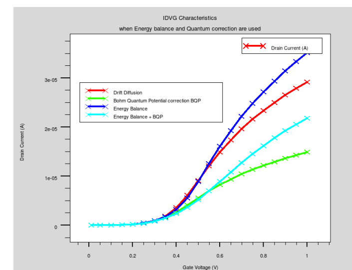
- Unstructured mesh to represent the structure
- Idealized isotropic and dry etching and planarization
- Selective etching or removal of materials regions
- Idealized conformal and direction deposition - Manhatten mode and curved mode
- Mask Layout-based Processing - Just like in a Fab
- Very fast empirical oxidation which approximates the oxide shape
- Deal-Grove and Massoud models are used in empirical mode



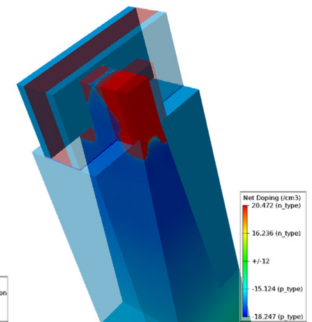
Fast analytical oxidation removes silicon and poly-silicon and adds an oxide layer.

Diffusion

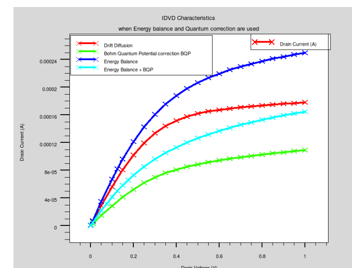
3D FinFET simulated including quantum correction and energy balance.



IDVG characteristics, simulated using Victory Device, showing the difference when energy balance and quantum correction are used.



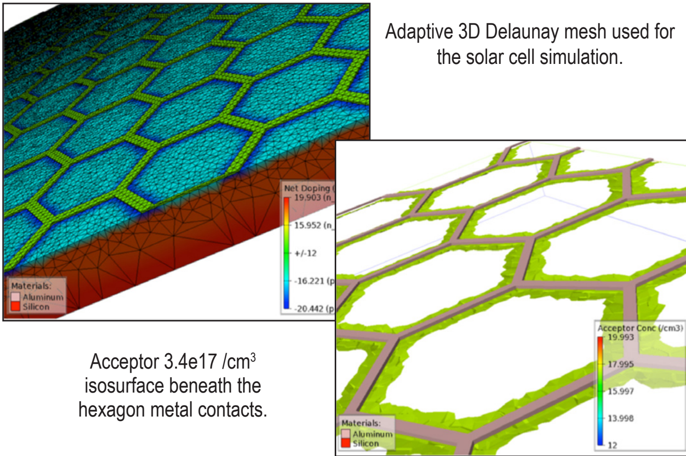
3D FinFET net doping distribution.



IDVD characteristics, simulated using Victory Device, showing the difference when energy balance and quantum correction are used.

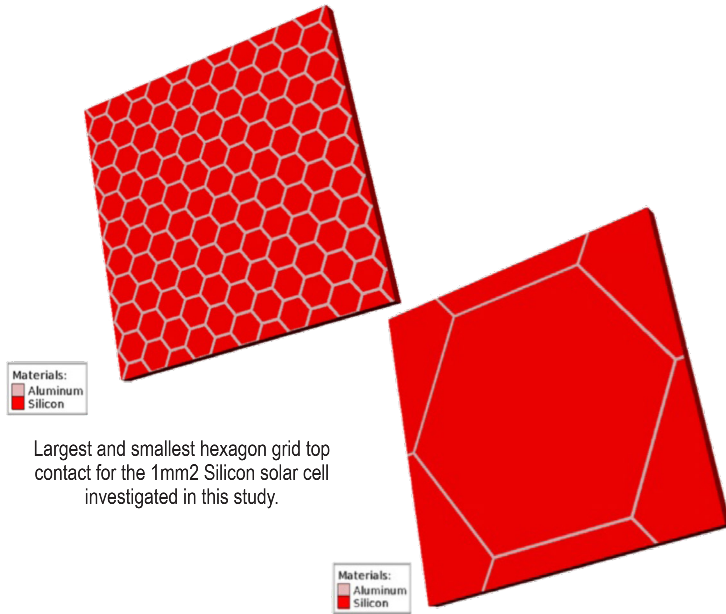
Optical – CIS, CCD, Solar Cells

Among the many design criteria for solar cells, the design of the top metal contact impacts the cell efficiency. The areal density of the top contact modifies the magnitude of the cell output power significantly.

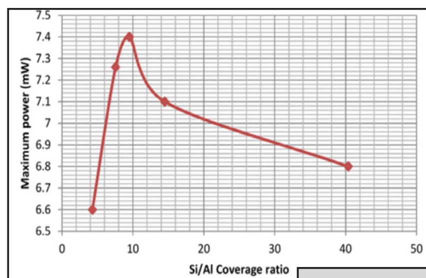


Adaptive 3D Delaunay mesh used for the solar cell simulation.

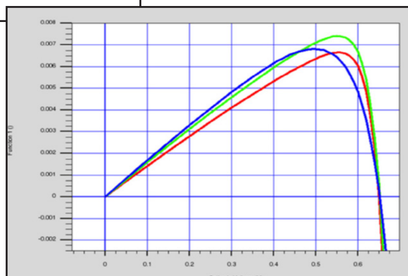
Acceptor 3.4e17 /cm^3 isosurface beneath the hexagon metal contacts.



Largest and smallest hexagon grid top contact for the 1mm2 Silicon solar cell investigated in this study.



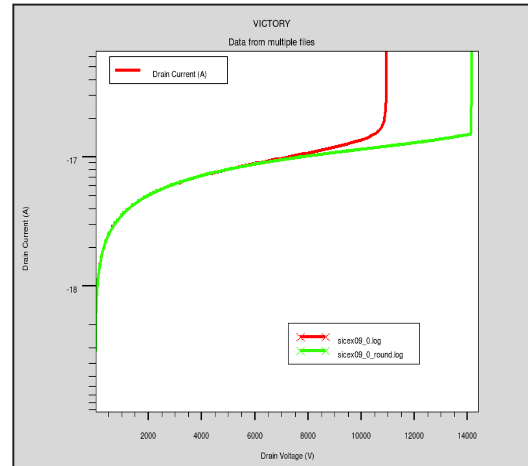
Showing the relationship between the maximum output power and the metal coverage ration R.



Solar cell efficiency with the red trace for the smallest hexagons (circumcircle radius or side length a of 104µm), green (a=225µm) and blue for the largest hexagon (a=945µm).

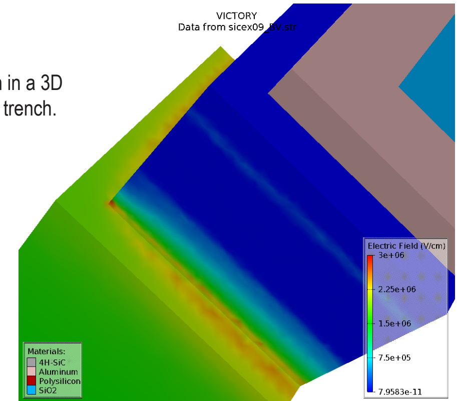
SiC Trench IGBT Example

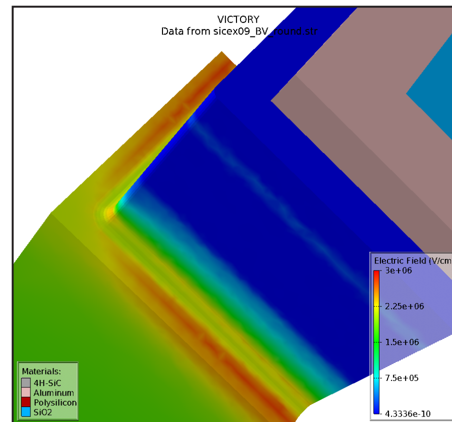
3D trench SiC IGBT simulation shows a ~350V increase in breakdown voltage for a rounded edge trench when compared to a sharp edge trench.



Comparison using Victory Device of 3D IGBT BV simulation results with sharp and rounded trench edges.

Electric field distribution in a 3D IGBT with sharp edge trench.

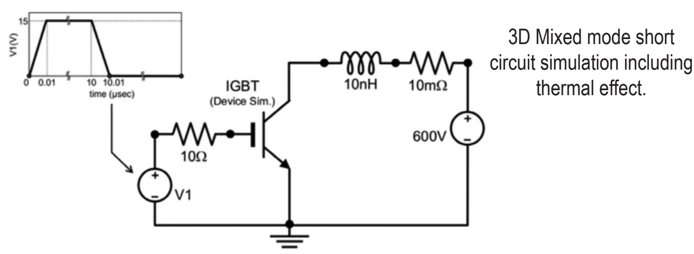




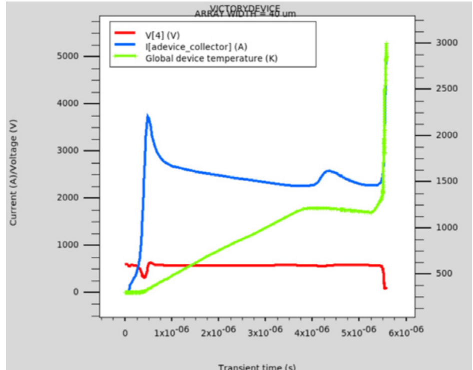
Electric field distribution in a 3D IGBT with rounded edge trench.

3D Current Crowding in Multiple Cells IGBT

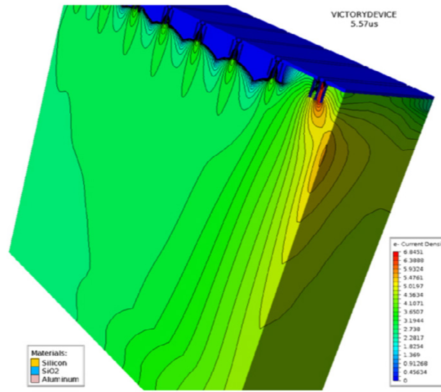
3D TCAD Mixed-Mode simulation of current filaments in IGBT multicell array under short-circuit condition.



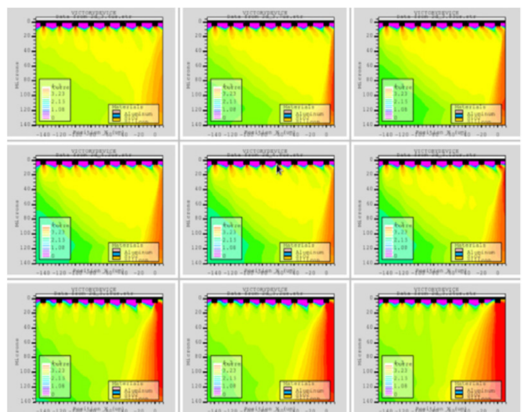
3D Mixed mode short circuit simulation including thermal effect.



Short-circuit waveforms for the 3D 8-cell IGBT array with a width of 40 µm.



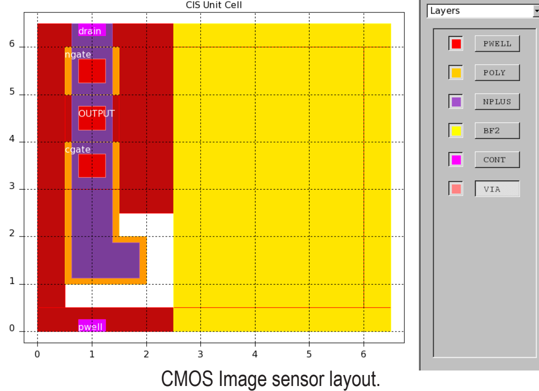
Electron current density distribution at device failure point t = 5.57 µs.



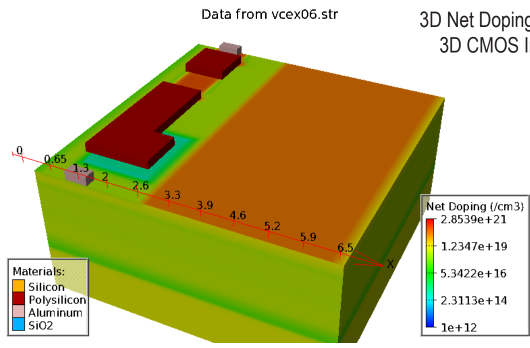
Short-circuit waveforms for the quasi-3D 8-cell IGBT array with a width of 1 µm (b) Cross-sectional views of spatial evolution of electron current density for selected points in time shortly before device burn-out.

CMOS Image Sensor Example

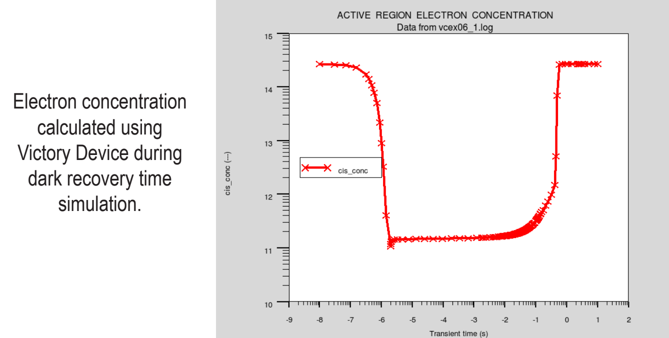
TCAD simulation of the full CMOS image sensor cell, including two pass transistors.



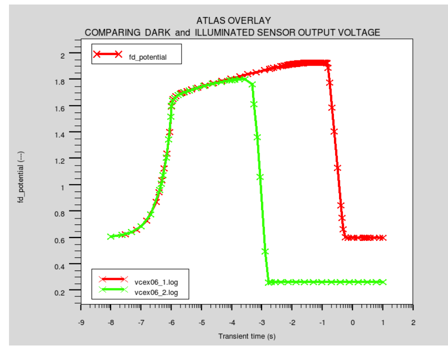
CMOS Image sensor layout.



3D Net Doping distribution in a 3D CMOS Image Sensor.



Electron concentration calculated using Victory Device during dark recovery time simulation.



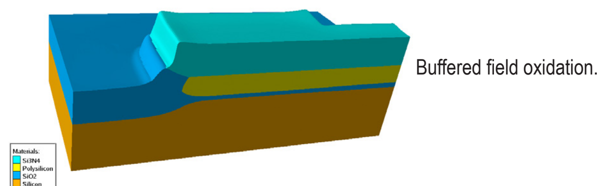
Comparison of sensor output voltage simulation using Victory Device without and under illumination.

Process Simulator Mode

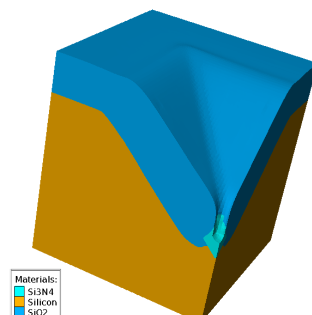
In process mode, the structure is represented implicitly, as a stack of material layers "sandwiched" between surfaces, each surface defined implicitly on the hierarchy of Cartesian meshes.

Oxidation Models

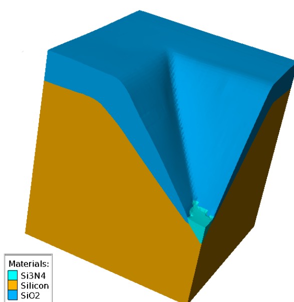
- Oxidation can be simulated in empirical, full physical, or hybrid mode
- Empirical mode is applied for very thin oxidation layers
- Deal-Grove and Massoud models are used in empirical mode
- Full physical mode simulates oxidant transport, reaction on Si/ SiO_2 interface, viscous flow, material deformation, and stress formation
- Automatic switching between empirical and full physical mode depending on oxide thickness
- Empirical mode is used in planar regions with coarse mesh allowing layer thicknesses smaller than mesh size to be resolved
- Full physical mode is used in regions with fine mesh
- Stress dependent oxygen transport and interface reaction
- Accounts for orientation dependence, doping dependence and ambient conditions
- Fully multi-threaded with run time reduction almost linearly proportional with number of CPUs
- Oxidation of compound semiconductors like SiGe and SiC also in heterostructure devices



Buffered field oxidation.



Without stress: local oxidation of a quarter section of an inverted pyramid shape using the default linear viscous model.



Stress dependent oxidation of an inverted pyramid. Stress occurs in corner regions. Retardation of the oxide growth due to stress becomes more significant closer to the apex due to the convergence of the corners.

Physical Etching and Deposition Module contains a comprehensive set of models covering a wide variety of topology evolution processes used in semiconductor fabrication and in hard coating for media and tribological applications.

Physical Etch

- Selective etching also with high selectivity
- Isotropic, anisotropic, and directional etching
- Crystal orientation dependent anisotropic etching (e.g., silicon in KOH)
- Plasma etching with material redeposition
- Accounts for particle transport effects and particle and reactor properties
- Multi-particle etching models like ion enhanced chemical etching for deep trench etching in memory technology
- Fully multi-threaded particle flux calculations with run time reduction almost linearly proportional with number of CPUs

Physical Deposit

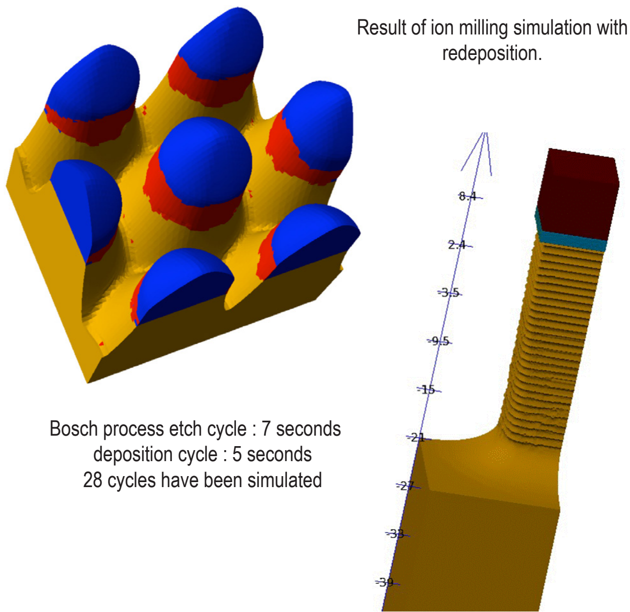
- Conformal, non-conformal, and directional deposition
- Sputter deposition
- Ion assisted sputter deposition
- Accounts for particle transport effects and particle and reactor properties
- Fully multi-threaded particle flux calculations with run time reduction almost linearly proportional with number of CPUs

Open Model Interface Capabilities

- Very fast empirical approximations for fluxes with multiple reflections
- User definable models for etch rates, conformity, anisotropy, and sticking coefficients
- User specified technological models (e.g., etch rate versus gas flow)
- User definable surface reaction models
- User definable particle transport characteristics through flux models
- All models account for ballistic transport
- Automatic selection of transport mode
- Transport and reaction of multiple particles

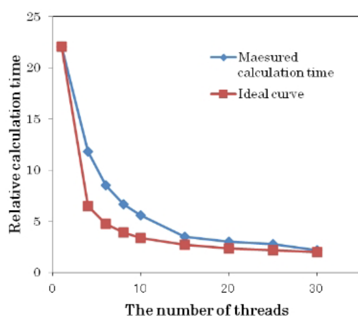
Ion Milling (IM) and Ion Beam Deposition (IBD)

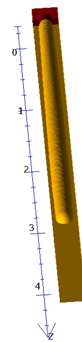
- Static and rotating beams
- Selective switching of rotating beams on and off including redeposition of multiple alloy materials
- Highly collimated and divergent beams for ion beam etching and ion beam deposition
- Capability to simulate re-depositon effects
- Configurable material specific yield functions and re-emission efficiencies
- Accounts for shading effects
- Empirical yield model taking into account processing conditions like ion energy, beam current, ion mass, ion charge



Result of ion milling simulation with redeposition.

Bosch process etch cycle : 7 seconds
deposition cycle : 5 seconds
28 cycles have been simulated





High aspect ration (1:30) trench etching with the ion enhanced chemical etching (IECE) model.

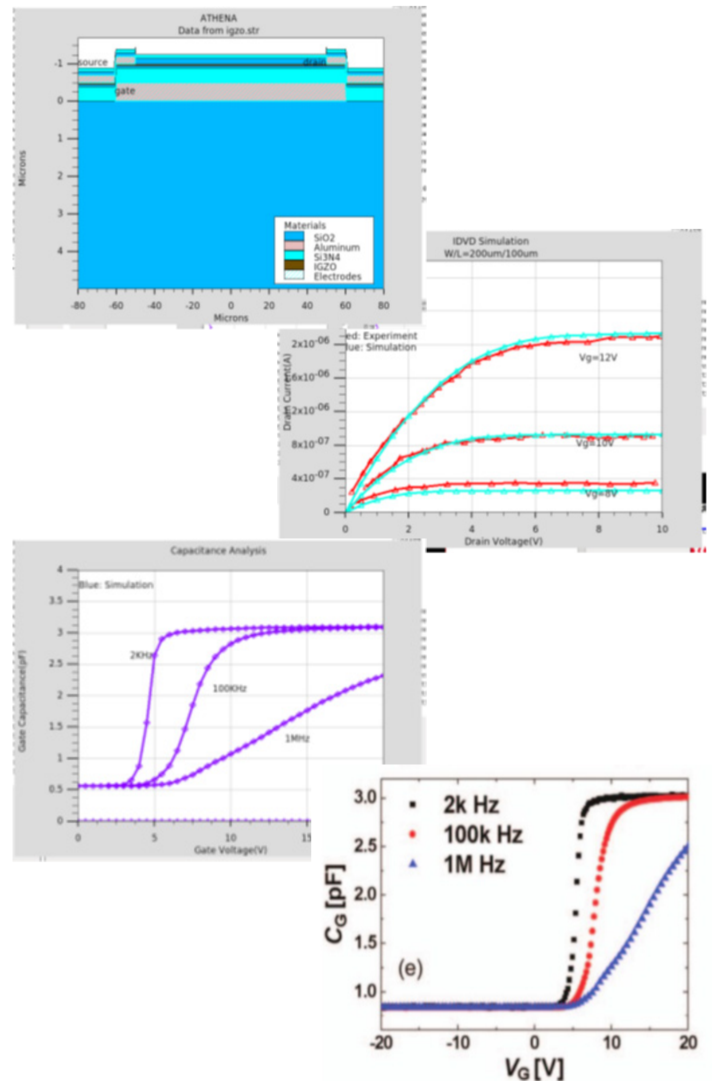
1D and 2D simulation capabilities are available in process mode. Can be considered as a direct replacement for Athena, with mostly compatible syntax for legacy input file conversion.

1D and 2D Mode

- Very similar syntax allows easy migration from Athena and T-Suprem
- Automated input deck conversion within Deckbuild
- Level-set based etch, deposit and oxidation, improves stability for complex structure shapes
- 1D/2D simulation allows quick calibration and process prototyping before full 3D simulation
- Open modeling interface and material database allow custom model development for standard and new materials and dopants
- Seamless link to Atlas and Victory Device
- Multi-threading for most time consuming process steps

a-IGZO TFT Characterization

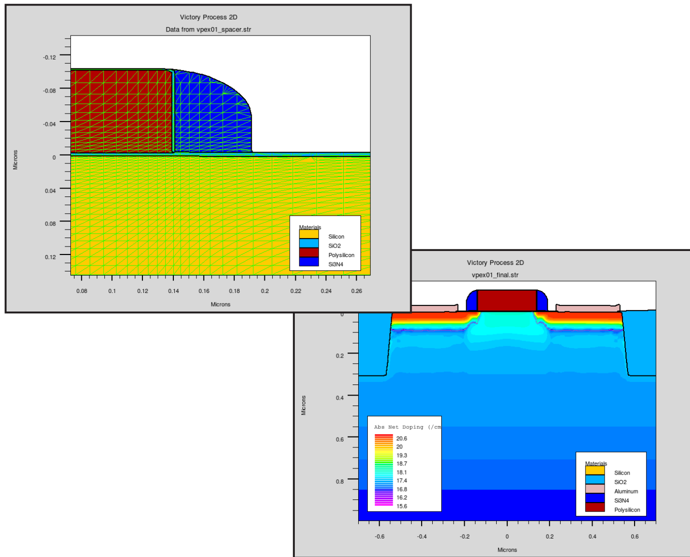
This example demonstrates coupled process and device simulation and characterization of an advanced amorphous InGaZnO thin film transistor used for display applications.



Structure of the a-IGZO TFT obtained by process simulation (left) and IV plot and IdVd plot obtained by device simulation compared to experiments.

28nm MOSFET

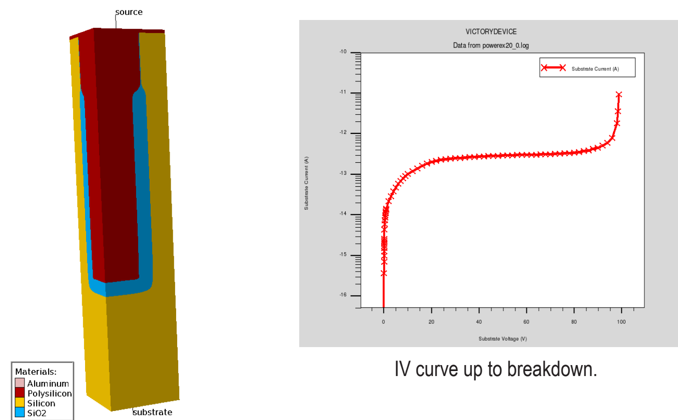
This example demonstrates 2D process simulation for 28nm NMOS transistor with STI (Shallow Trench Isolation). The goal of this example is to demonstrates generic compatibility with Athena.



2D process simulation results after 20 process steps including etching, deposition, ion implantation and diffusion/oxidation.

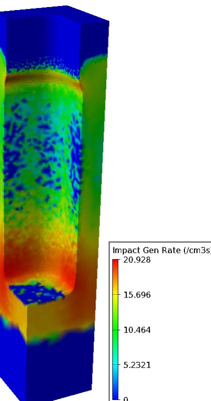
3D Vertical LOCOS Power MOSFET

This example shows a 3D curved corner vertical LOCOS MOS power device created by a simplified process flow in Victory Process. The structure is then exported to Victory Device for electrical simulation.



Geometry of the vertical MOSFET.

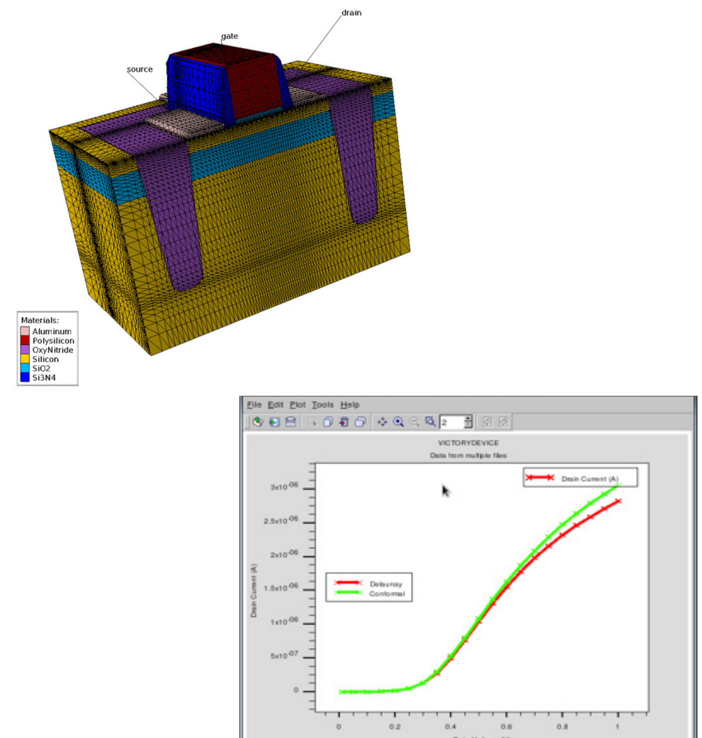
IV curve up to breakdown.

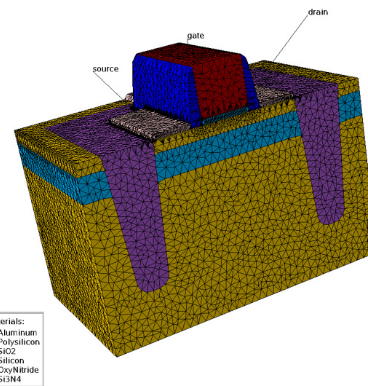


Impact ionization rate near breakdown.

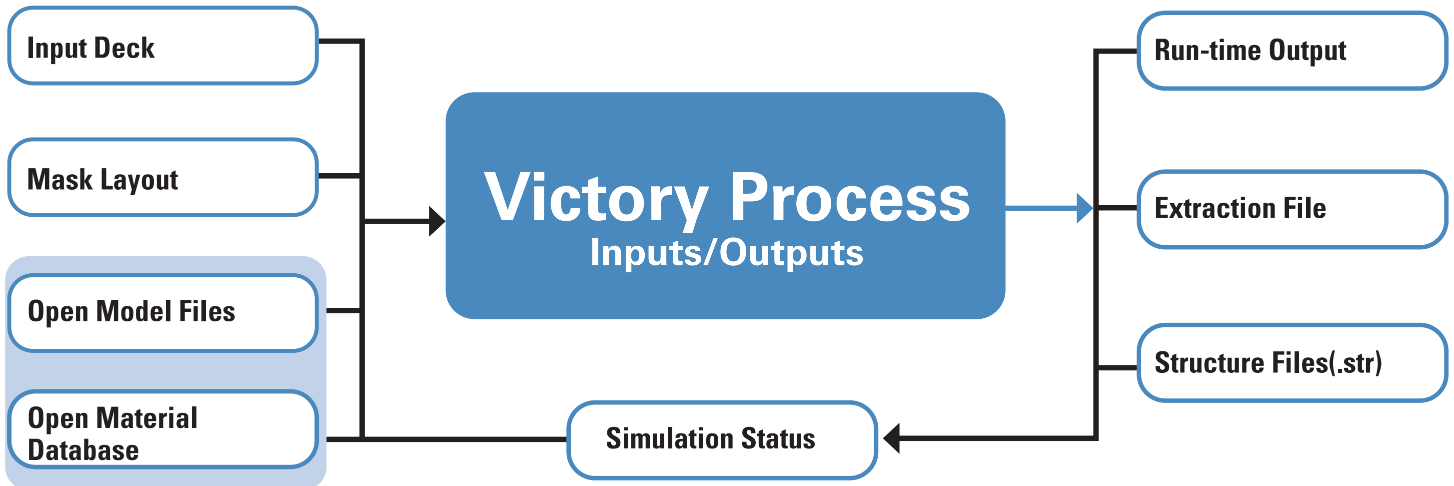
20 nm FDSOI

Coupled process and device simulation of narrow 20 nm fully depleted SOI transistor using different device meshing methods.





Analysis of the impact of the mesh shape on the saturation current (top- Victory (conformal) mesh, middle - Victory (delaunay) mesh, bottom - IV curve obtained with different device meshes)



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