SmartDRC/LVS with SmartRDE

Smart Physical Verification

SILVACO

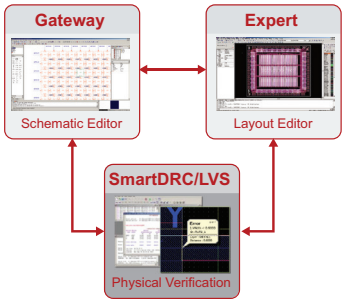
SmartDRC and SmartLVS with SmartRDE deliver physical verification of analog, mixed signal, and RF IC designs with high performance and accuracy. Tightly integrated with Silvaco's schematic capture and layout editor, SmartDRC/LVS efficiently performs design rule checks (DRC), electrical rule checks (ERC), layout vs. layout comparison (LVL), fill layer generation, layout netlist extraction, and layout vs. schematic (SmartLVS) comparisons.

Key Features

- Can work either in standalone mode or as a part of Silvaco Analog Custom Design Flow
- Integration with Gateway schematic capture, Expert layout editor, full custom design ecosystem, and other third-party layout tools for increased productivity
- SmartRDE reduces debugging time with intuitive and powerful debugging tools
- Innovative One-Shot™ layout scanning technology ensures near-linear scaling and runtime predictability
- Broad support (including sign-off) of semiconductor process technologies through foundry-proven process design kits (PDKs)
- Fast, intuitive, and hierarchical LVS debugging with cross-probing to layout and schematic views
- SmartLVS Supports stress effects and well proximity parameter extraction
- Performs layout vs layout layer-by-layer comparison or hierarchical Quick Diff (LVL) to supply ECO
- Silvaco's strong encryption is available to protect valuable customer and third-party intellectual property

SmartDRC

- Full DRC command set for every design both for interactive usage with SmartRDE GUI and in batch mode
- Hierarchical processing of big macro blocks and cell arrays that can be enabled on demand
- Optional hierarchical reports in sign-off mode
- Optimized layer operations based on efficient memory management and advanced algorithms get the most performance from Windows and Linux platforms
- Connectivity-based DRC operations including antenna rule checking
- Optimized execution of DRC commands using block-based rule processing
- Output results are compatible with industry standards



SmartDRC/LVS Tightly Coupled with Silvaco Analog Custom Design Flow
Easily Integrates with 3rd-Party Design Flows

SmartLVS

- Intuitive hierarchical LVS mismatch report significantly decreases time for error debugging
- Advanced capabilities for device parameters extraction and comparison
- Direct database links between Gateway Schematic and Expert Layout Editors with cross probing option
- Black-box options for subcircuits provides incremental LVS comparison in hierarchical mode and easy inclusion of IP blocks into the verified design at the top level

SmartRDE

- Manage run settings with on-the-fly validity checks
- Start DRC, LVL, LVS or pure NVN jobs while monitoring their progress
- Sort DRC violations by rules or by cells
- Filter DRC results by area
- Filter LVS results by cells, nets and devices types
- Interactively debug with layout editor of choice
- Check logs and other reports
- Waiver capability to aid processing
- View and debug your LVS results from Extraction

SmartDRC/LVS Rule Language

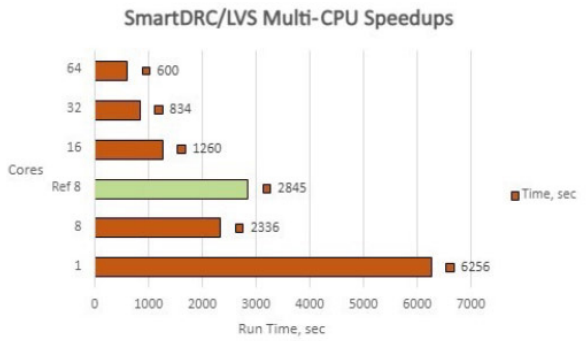
- PWRL (pronounced Power-L)
- Rich set of checks and operations
- Flexible due to preprocessing tools like variables, conditionals, macros, and includes
- Easy to learn and use
- Allows for full or partial rules encryption
- Compile Only mode of SmartDRC/LVS allows for rule file debugging
- Wide availability of rules/PDKs for various processes

Speed, Accuracy and Capacity

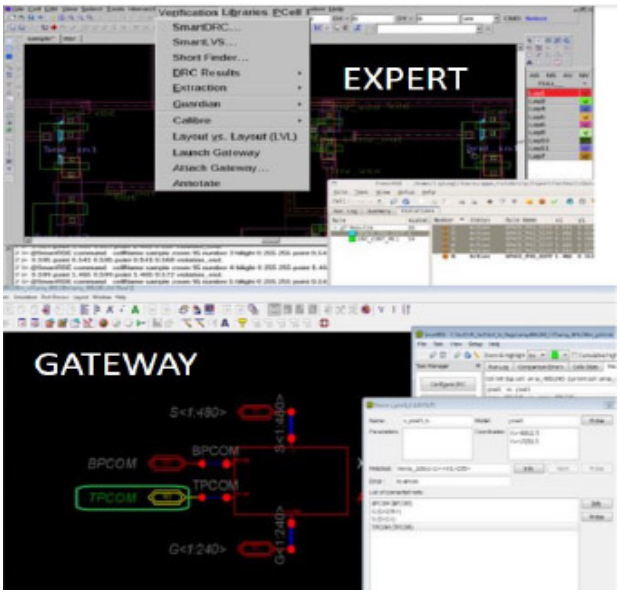
- Parallel DRC tasks may be run in multi-CPU mode on:
  - o A single multi-core host
  - o Multi-host virtual machine
- Scalability proven with up to 128 CPU cores
- SmartDRC benefits from parallel processing of:
  - o Independent groups of rules (blocks)
  - o Independent parts of layout (strips)
  - o Independent macro blocks (in hierarchical mode)
- Precise recognition of built-in devices (transistors, diodes, resistors, capacitors, etc.), user-defined generic devices, user-defined subcircuits and/or black-box subcircuits during LVS trace
- Efficient full-chip layout netlist extraction for any semiconductor planar process with extremely predictable performance
- Accuracy and Capacity to handle Flat Panel Displays
- Accurate calculation built-in device parameters
- Accurate calculation of geometry-dependent device properties that are important for analog design with built-in or user-defined equations and macros

Productivity and Versatility

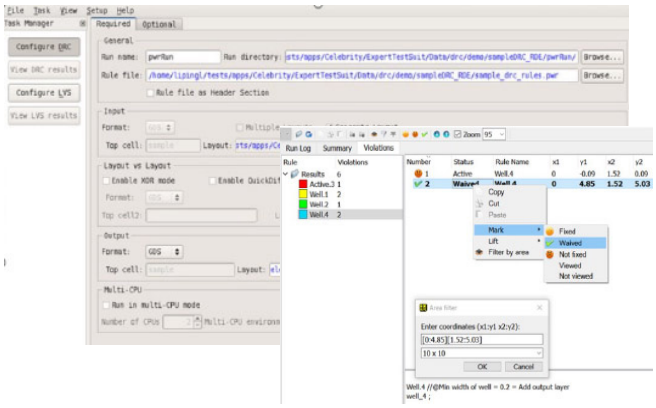
- Hierarchical design database supports operations for flat and hierarchical LVS netlist comparison
- Handles any arbitrary shaped (any-angled) polygon geometry used in device formation
- Hierarchical cross-probing of schematic netlist, extracted layout netlist, schematic design, and physical layout with convenient filtering options
- Detects and highlights ERC violations (shorts, opens, floating nets, virtual connects and malformed devices)
- Flat , hierarchical or blackbox Netlist Vs Netlist comparison
- Compile Schematic option for netlist debugging
- Formats supported:
  - o Layout: GDS, OASIS, and OA
  - o Schematic: SPICE, CDL, Verilog and OA
- Supported platforms: Windows, Linux



4 x Intel Xeon E5-2686 2.3GHz (64 CPU cores)
RAM: 128 GB, HDD: 10 GB SAS + 150 GB



LVS cross-probing: Interactive hierarchical cross-probing of LVS discrepancy is clearly displayed



Configure DRC run and View DRC results with SmartRDE

SILVACO
HEADQUARTERS
4701 Patrick Henry Drive, Bldg #23
Santa Clara, CA 95054

NORTH AMERICA sales@silvaco.com
BRAZIL br_sales@silvaco.com
EUROPE eusales@silvaco.com

JAPAN jpsales@silvaco.com
KOREA krsales@silvaco.com
TAIWAN twsales@silvaco.com
SINGAPORE sgsales@silvaco.com
CHINA cn_sales@silvaco.com

WWW.SILVACO.COM

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