Cello

Cell Library Migration and Optimization

SILVACO

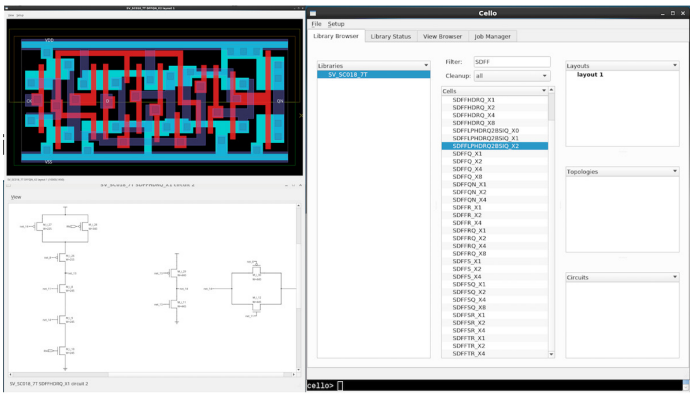
Overview

Silvaco Cello™ is the industry's versatile, integrated, and easy-to-use solution for digital cell library migration and optimization. It enables designers of digital CMOS ICs to custom-tailor digital cell libraries and explore the impact of alternate device models, design rules, and cell architectures, as well as process migration.

With Cello, designers can control and alter the individual attributes of all digital library cells, making precise adjustments to cell parameters to fulfill the strictest design requirements.

For example, transistor sizing strategy and row height can be set to control the trade-off between power usage, frequency, and area. The user can balance DFM trade-offs between recommended and required rules, thus optimizing layout yield without an increase in the total cell area.

Cello contains the full set of tools needed to optimize and migrate standard cell libraries. It complements existing design flows and provides all of the outputs required by the physical synthesis tool chain.



Key Benefits:

- Eliminate or significantly reduce layout manual effort
- Significantly improve productivity
- Consistent layout, correct by construction including pin access and block abutment
- Enables exploration of different dimensions (cell architecture, design rules, sizing strategy, DFM rules)
- Migrate layouts between cell architectures, technology nodes or foundries
- Easily expand your portfolio of libraries
- Reuse layouts
- Interactive layout cleanup and optimization
- Structured workflow: 2-week ramp-up for new Layout Engineers

Key Features:

- Fast setup of process technologies and foundry design rules, enabling DRC clean layout generation in the first week of use
- Advanced process technology, including context sensitive spacing and enclosure rules, preferred shape patterns, self-aligned double patterning (SADP) and support of local interconnect
- Scalable parallel processing to improve throughput
- Integration with leading third-party DRC, LVS and LPE tools to ensure high-quality sign-off layouts and minimal disruption to customer existing flows
- Generate footprint-compatible cells starting with GDSII or automatically generated layouts to create fine-grained drive and skew variants, enabling late-stage speed and power optimization
- TCL scripting support provides the flexibility to customize the layout flow.
- Cadence Virtuoso plugin

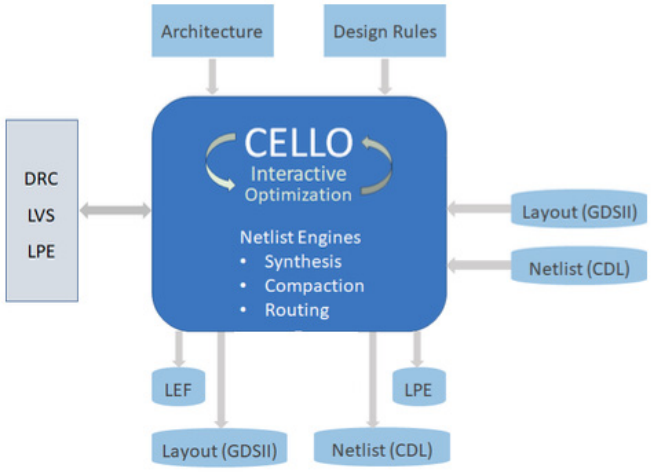
Advanced Layout Migration Flow

- Uses cell templates to configure predefined shapes, routing parameters, track height, gate pitch, P/N ratios, size and position of power rails, etc.
- Resizes transistors to satisfy new template or drive strength requirements, also allowing creation of gate length variants required for low leakage applications
- Supports wide range of layout migration methodologies including equation-based input to GDS-based layout migration, depending on how much the layout must be stripped from its characteristics, supporting a broad range of applications
- Full scripting interface support provides the flexibility to integrate Cello into existing design flows and to perform design goal searching through iterative loops

Completeness

Fully automated layout topology generation using advanced optimization algorithms that minimize cell area and parasitic effects. Optimization strategies include:

- Optimal cell input sequencing
- Optimal diffusion strip layout
- Transistor netlist synthesis with built-in transistor sizing algorithms and override options including logical effort
- User-definable topology generators with support for an advanced parameterized set of layout primitives:
  - Contact and contact arrays
  - Single and folded transistor configurations
  - Routing preferences and pattern restrictions/allowances
  - Input and output port guidance and blockages
- Advanced proprietary compaction engine:
  - Adaptive topology-driven compaction strategies
  - Full design rule support for advanced CMOS processes as well as user constraints
- Scalable parallel execution of SPICE simulations and layout generation through:
  - SUN® Grid Engine (SGE)
  - Multi- and single-threaded processing
- Built-in verification, including:
  - Formal equivalency checking of layout function vs. Boolean definition
  - Interface to external physical verification for independent QA
  - DFM analysis and scoring through external verification tools



Digital Cell Types

- Buffers (inverting, non-inverting, clock)
- Boolean combinational (AND, OR, NAND, NOR, AOI, OAI, OA, AO, MUX)
- Arithmetic (XOR, full-adder, half-adder)
- Sequential (latches, clock-gates, D-type flip/flops with any optional combination of scan input, set, and reset)
- Miscellaneous (tie cells, filler cells, antenna, diode, ECO gates)
- User-defined complex gates based on Boolean equations
- User-defined cells from SPICE netlists
- Power Management (level-shifter, header, footer and always-on cells)

Inputs

- Silvaco technology file containing foundry design rules
- SPICE netlist
- GDSII

Outputs

- LEF (Library Exchange Format)
- GDSII (Graphics Design System II) cell layouts
- Cell schematics

Platform Support

- Red Hat Enterprise Linux® version 6 and 7 (x86 or x86-64)

SILVACO
HEADQUARTERS
4701 Patrick Henry Drive, Bldg #23
Santa Clara, CA 95054

NORTH AMERICA sales@silvaco.com
BRAZIL br_sales@silvaco.com
EUROPE eusales@silvaco.com

JAPAN jpsales@silvaco.com
KOREA krsales@silvaco.com
TAIWAN twsales@silvaco.com
SINGAPORE sgsales@silvaco.com
CHINA cn_sales@silvaco.com

WWW.SILVACO.COM

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