Cello FinFET

Automated Cell Library Creation and Optimization

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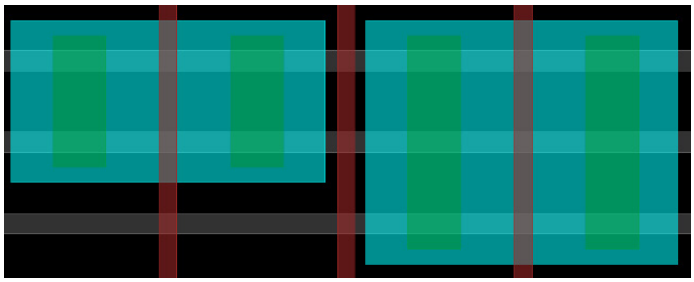
Overview

Cello FinFET is a versatile standard cell library creation and optimization tool. It reads schematic netlist in and generates correct-by-construction standard cells. Cello FinFET is an easy-to-use solution for automated FinFET-based digital cell library creation and optimization. It enables designers of advanced geometry digital CMOS ICs to custom-tailor digital cell libraries and explore the impact of alternate device models, design rules, and cell architectures, as well as optimization.

With Cello FinFET, designers can control and alter the individual attributes of all digital library cells, making precise adjustments to cell parameters to fulfill the strictest design requirements.

Using the built-in routing engine, transistor sizing strategy and row height can be set to control the trade-off between power usage, frequency, and area. The user can balance DFM trade-offs between recommended and required rules, thus optimizing layout yield without an increase in the total cell area.

Cello FinFET is a complete stand-alone tool that can automatically create and optimize standard cell libraries.



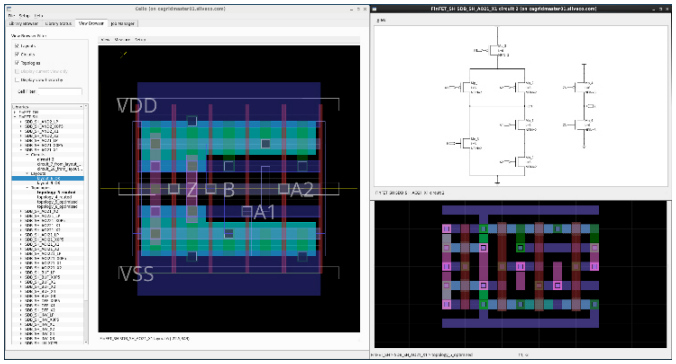
FinFET Transistors

Key Benefits:

- Significantly improves productivity
- Eliminates or greatly reduces manual layout effort
- Fast turnaround time, complete library in one day
- Enables exploration of different dimensions (cell architecture, design rules, sizing strategy, different track heights, DFM rules)
- Consistent layout
- Reuse of schematics reduces design time
- Automates PDK updates

Key Features:

- Sub-10nm FinFET support
- Integrated place and route engine creates correct by construction layout
- Compatible with multi-patterning rules, cut rules, or any other complex FinFET processes rules
- Advanced process technology, including context sensitive spacing and enclosure rules, preferred shape patterns, self-aligned double patterning (SADP) and support of local interconnect
- Scalable parallel processing to improve throughput
- Multiple layout options are created simultaneously
- Integration with leading third-party DRC, LVS and LPE tools to ensure high-quality sign-off layouts and minimal disruption to existing flows
- Flexible setup of process technologies and foundry design rules, enabling ultra-fast, DRC clean layout generation



Cello FinFET

Advanced Layout Automation Flow

- Compatible with all design rules
- Correct by construction
- Supports both single and double-height cells
- Minimize area, maximize abutted diffusions, minimize wirelength, and prioritize net length
- Prioritize and minimize net length
- Explore different folding configurations
- For dual-height cells: maximize poly alignment and diffusion alignment across both metal halves

Increase Productivity

- Based on just a schematic netlist input, Cello FinFET delivers fully automated layout topology generation using advanced optimization algorithms that minimize cell area and parasitic effects.
- Reduces library development time by up to 80%
- Maximizes your limited resources
- Reuses existing schematics for new layout architectures
- Enables fast exploration of different dimensions (cell architecture, design rules, sizing strategy, DFM rules)

Inputs

- Technology file containing foundry design rules
- Configuration file describing cell architecture
- SPICE netlist

Outputs

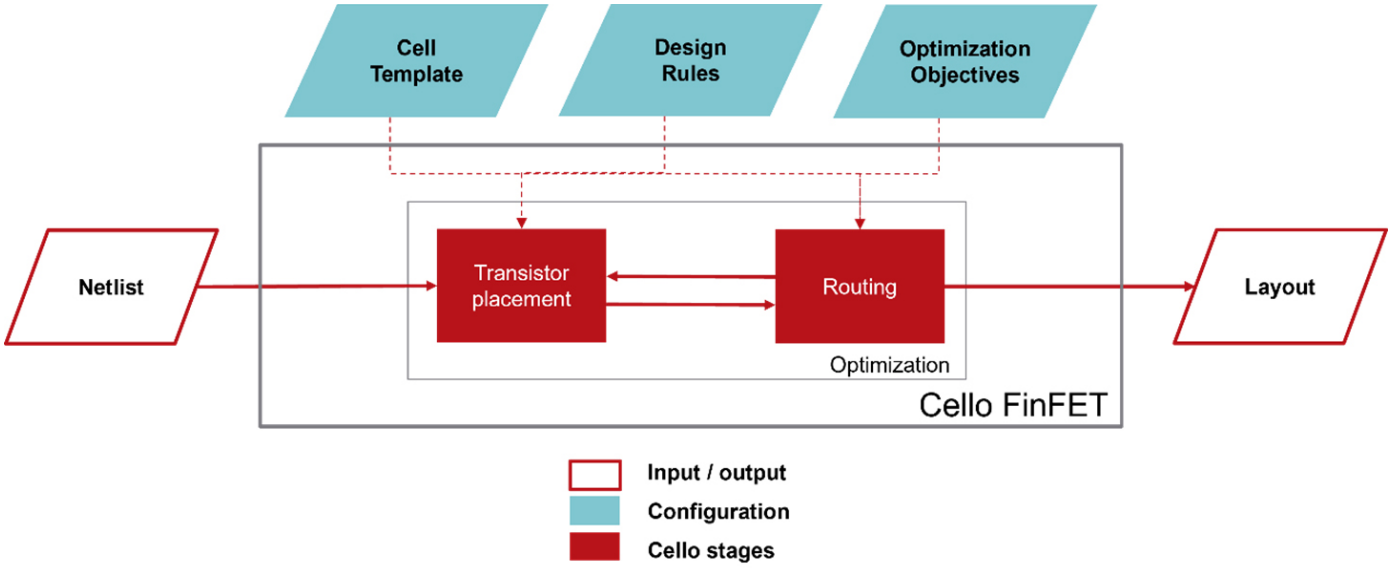
- GDSII (Graphics Design System II) cell layouts
- LEF (Library Exchange Format)

Optimize Layout Strategies

- Obeys all design rules simultaneously
- Promotes uniform quality
- Enables design space exploration
  - Richer cell libraries
  - Different layout styles
  - Multiple track heights
  - Different cell architectures
  - Multi height implementation
  - Different folding configurations
- Targets sub-10nm nodes
  - Supports any technology
  - FinFET, GAA, nanosheet, etc.

Platform Support

- Red Hat Enterprise Linux® version 6 and 7 (x86 or x86-64)



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