# Ultra High-Speed Cache Memory Compiler
# 2-Port Register File
# TSMC N3P

SILVACO

## Overview

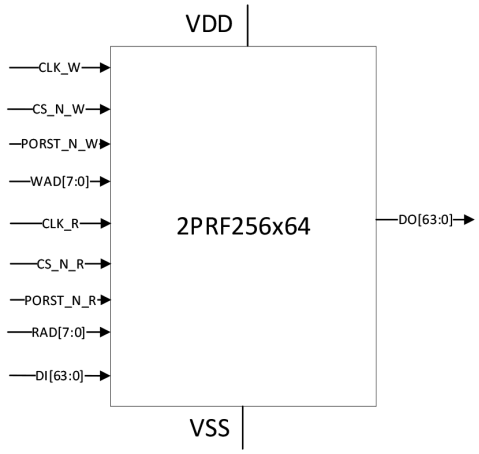
Silvaco's Ultra High-Speed cache memory is an adaptable, independent, non-coherent cache Intellectual Property (IP) featuring an advanced cache architecture. This architecture enhances system performance, scalability, power efficiency, data locality, application responsiveness, cost optimization, and market competitiveness, providing a distinctive business value.

## Highlights

- Up to 3.4 GHz operation in N3P process
- Cache size up to 16 Kb
- 4 – 64-bit word width
- Configurable way associativity
- Custom logic-rules bitcell
- Speed / Static Power tradeoff option

## High Performance SoC Challenges

Contemporary System-on-Chip (SoC) design faces challenges in optimizing data sharing between compute engines, accelerators, and other data processing blocks. Efficient data prefetching mechanisms are essential to minimize reliance on main memory accesses. Meeting these requirements is crucial for achieving performance goals at both the block and SoC levels.




## Silvaco Cache Solution

Silvaco's Ultra High-Speed cache memory is versatile in its application across various scenarios within computer systems. Its primary objective is to optimize system performance by mitigating memory access latency. This is accomplished by storing frequently accessed data in proximity to the processing cores, enabling swift retrieval. Functioning as a shared cache, it facilitates smooth communication and synchronization among components or Intellectual Properties (IPs).

The memory serves as a transient storage and buffering mechanism for data in transit, facilitating effective data flow management. Caching frequently accessed data diminishes the necessity to access the slower main memory, leading to an overall improvement in system responsiveness. Consequently, this enhances power efficiency by reducing both memory access frequency and the associated power consumption.

## Compiler Flexibility

| Memory Capacity Range: 32-bits to 16k-bits | | | | |
|---|---|---|---|---|
| Mux Size | Address Range | Address Increment Step | Word Width (bits) | Word Width Increment Step |
| 1 | 8-256 | 1 | 4-64 | 1 |

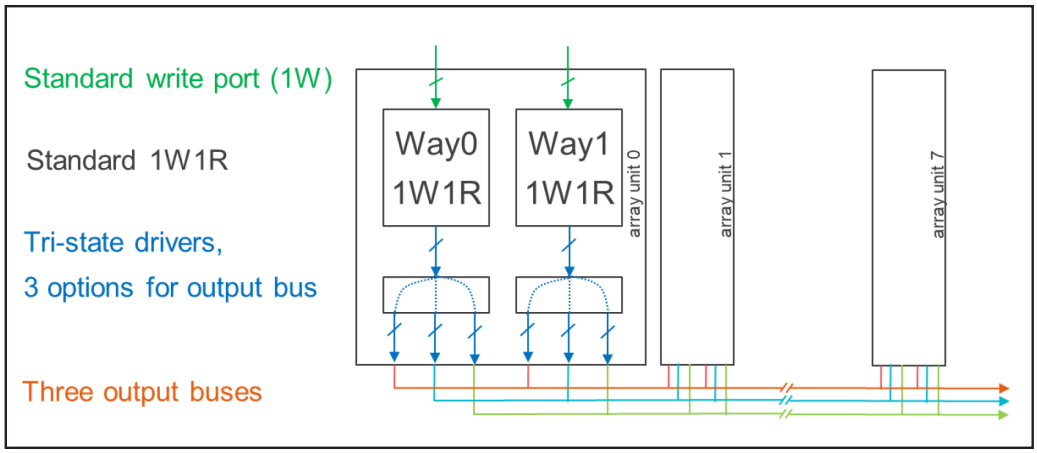
## Cache Types

- Data array
- Instruction array
- Virtual tag array
- Physical tag array, PTAG

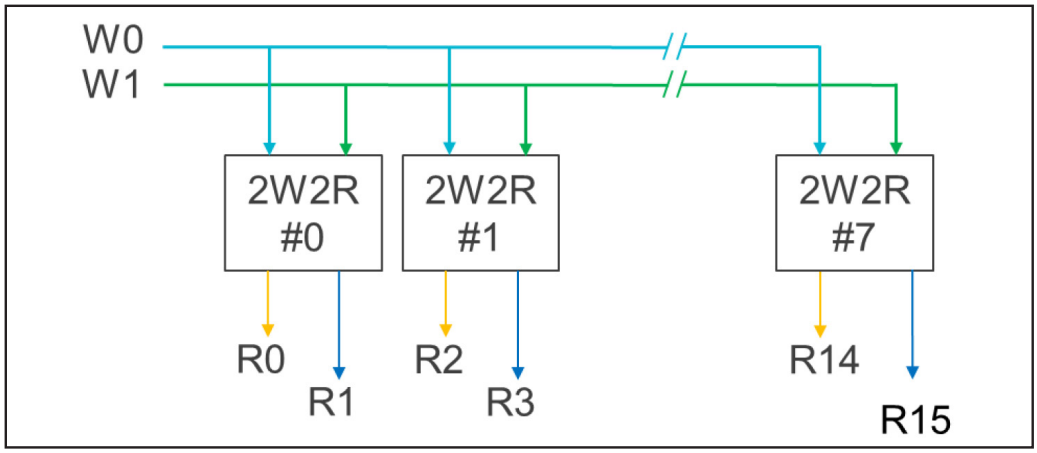
## Cache Applications

- AI Processors
- Data Center
- High Performance Computing
- Network Compute Units
- Neural Processor

## 2-Way 1-Write, 1-Read Data Array Example




## 16-Way 2-Write, 16-Read PTAG Array




Performance, area, and power specifications are available upon request.