AHB Performance Subsystem - ARM Cortex M0

SILVACO

The AHB Performance Subsystem is an AMBA® based system that is useful as the digital infrastructure for building low power SOCs needing additional performance. This AHB Multi-matrix system contains a flexible Power Management Unit for controlling power sequencing of the CPU and peripherals. The PMU can easily be extended to control additional cores, peripherals and even analog subsystems on the same SOC.

Additionally, the subsystem includes four DMA controllers for easily moving data from user peripherals to internal SRAM.

This subsystem is a good choice for IoT devices where computation has to be done at the edge.

The AHB Performance Subsystem includes a standard set of peripherals and cores that supports RTOS and software kernels. Included is a QSPI, serial flash controller for boot loading program images or operating as an Execute in Place (XIP) engine using nonvolatile external flash memory with low power.

The AHB Performance Subsystem is soft IP that can be used in all the popular semiconductor technology nodes.

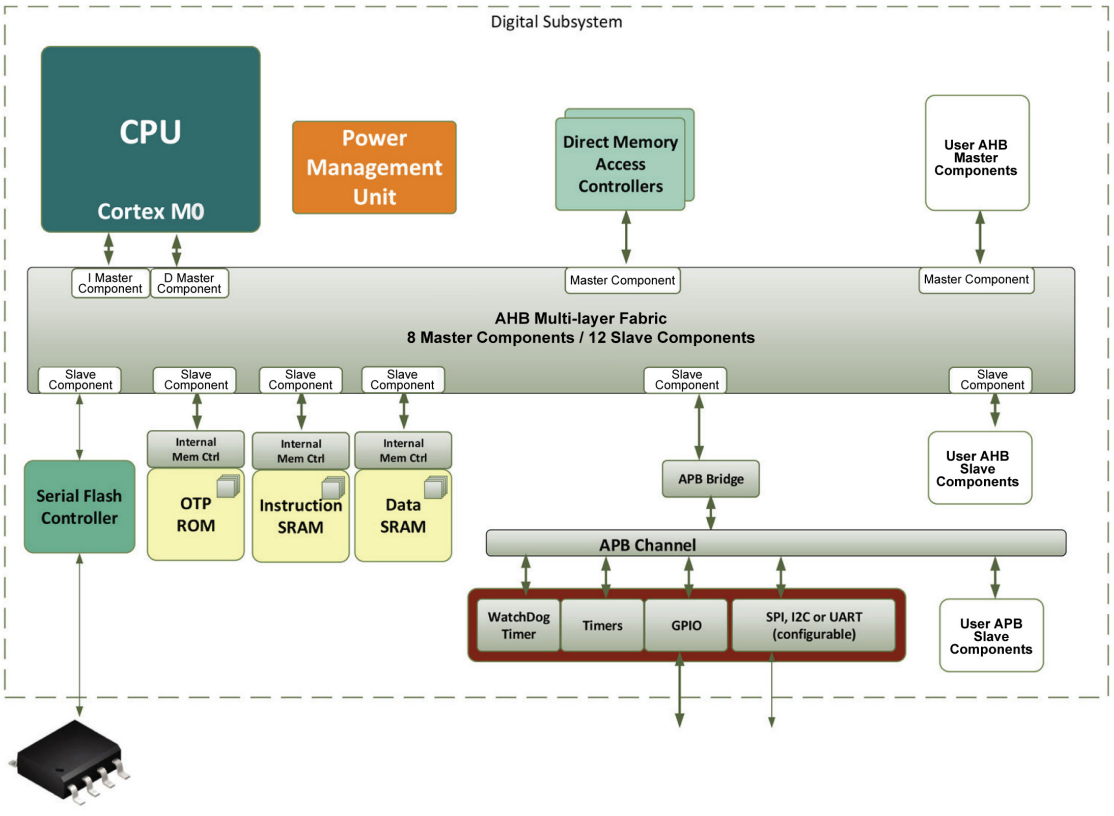
Features

- High Performance with Low Power
- RTOS/Kernel Support
- AMBA AHB 2.0 Multi-layer Fabric
- AMAB APB 3.0
- Power Management Unit

Applications

- IoT Edge Devices
- Medical Devices
- Mixed Signal Digital - MEMS
- Smart Sensors, Smart Metering, Smart Lighting
- Health Monitors
- Home / Office
  - Surveillance, Home Automation, Smart Thermostats
- Industrial
  - Machine / Motor Control, System Health Monitoring

AHB Low Power Subsystem – ARM Cortex M0



Processor Options

- ARM Cortex-M0

Infrastructure

- AHB Multi-layer Fabric
- 8 Master components – 12 Slave components
- APB 3.0 Bus Channel / Decode
- AHB to APB Bridge (2)

IP Cores

- 8, 16, 32-bit Internal SRAM Controller
- DMA Controller (2)
- QSPI Serial Flash Controller with Execute in Place (XIP)
- Watchdog Timer
- Timers (2)
- General Purpose Input / Output (GPIO)
- I2C Master/Slave components
- QSPI / SPI components
- 16550 UART
- Remap register
- Generic Registers

Software

- Startup and Interrupt code
- Example Boot Loader from QSPI Serial device
- Example test code for all IP Cores
- Low power example project

Deliverables

- Verilog RTL source code
- Test bench with test suites
- Documentation including User's Guide and Integration Guide
- Technology-independent synthesis constraints
- C software example projects

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