AHB Channel with Decoder and Data Mux IP Core

The AHB Channel provides the necessary infrastructure to connect as many as 7 AHB Slave components (numbered 1-7) to an AHB bus Master component. The AHB Channel performs a combinational decode on the incoming AHB address to produce the block selects for the various AHB Slave components. The address decoder contained in the AHB Channel has one area of memory reserved for a configurable remap application.

Typically, the AHB Channel is connected as in the following description. Each of the AHB Channel's 7 Mirrored Slave component Ports is connected to an AHB Slave component module (e.g. External Bus Interface, Memory Controller, AHB-to-APB Bridge.) On the Master component side, the AHB Channel's Mirrored Master component Port is connected either to an AHB Arbiter (in an AHB system with multiple bus Master components) or directly to an AHB Master component such as a micro-processor (in an AHB system with a single bus Master component.)
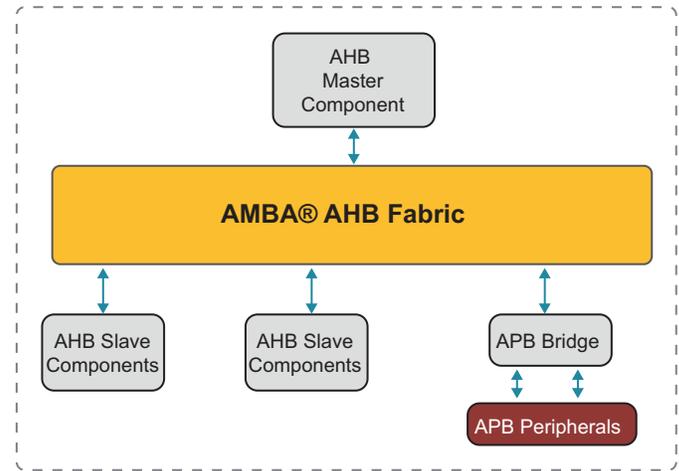
Features

- AMBA® 2.0 Compatible
- Simple AHB Infrastructure for up to 7 AHB Slave components
- Multiple Master component can be easily accommodated using AHB Arbiter
- Includes Address Decoding
- Includes Read Data Muxing
- Remap to assist boot loading and debug

Deliverables

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model

For more information, please contact us at ip@silvaco.com.