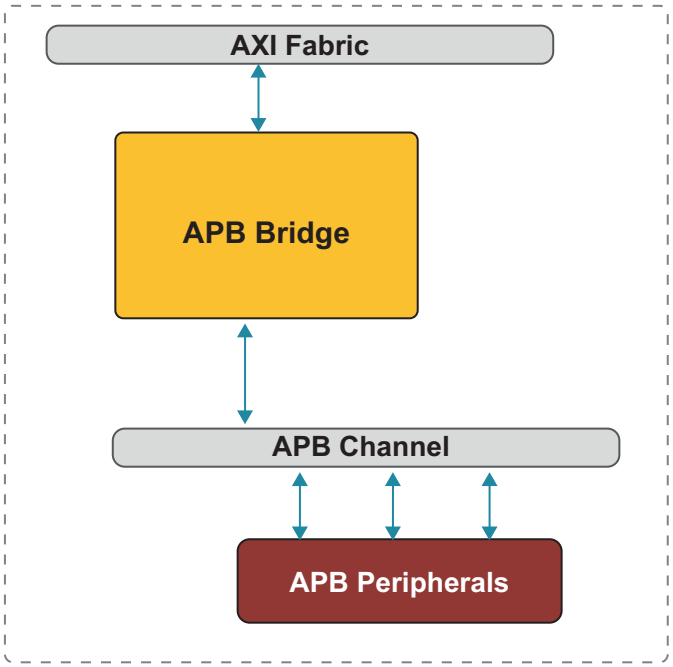
AXI to APB Bus Bridge

The AXI to APB Bridge translates an AXI bus transaction (read or write) to an APB bus transaction. This is accomplished via two state machines – one governing the AXI transactions, and one governing APB transactions.

The AXI to APB Bridge acts as an AXI Slave component, and an APB Master component in an AXI/APB subsystem. Typically, the AXI to APB Bridge has its AXI interface connected to a Slave component port on an AXI Channel/Interconnect module, and its APB interface connected to the Master component port on an APB Channel module.



Features

- Translates AMBA® AXI transactions to APB transactions
- Low latency
- Low Gate Count
- Supports APB 2.0 and APB 3.0 Signaling
- Independent ACLK, PCLK pseudo-synchronous clocks

Deliverables

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model

For more information, please contact us at ip@silvaco.com.

SILVACO
HEADQUARTERS
4701 Patrick Henry Drive, Bldg #23
Santa Clara, CA 95054

NORTH AMERICA sales@silvaco.com
BRAZIL br_sales@silvaco.com
EUROPE eusales@silvaco.com

JAPAN jpsales@silvaco.com
KOREA krsales@silvaco.com
TAIWAN twsales@silvaco.com
SINGAPORE sgsales@silvaco.com
CHINA cn_sales@silvaco.com

WWW.SILVACO.COM

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