ColdFire® V2 Core

SILVACO

The ColdFire V2 Core (CFV2CORE) is a small, yet powerful implementation of the ColdFire architecture, offering over 250 DMIPS of performance at 240 MHz using as few as 40K gates. Tightly-integrated arithmetic hardware, including a divider and optional enhanced MAC (EMAC), provide faster execution of multiply instructions and support DSP-like algorithms for applications such as voice-over-IP.

Like all ColdFire processor cores available from Silvaco, the ColdFire V2 Core is a production-proven design. The ColdFire V2 Core is the same IP implemented in NXP MCF52xx devices. And, like the ColdFire V1 and V4 cores, the ColdFire V2 Core benefits from the extensive ecosystem of development systems, tools, and software supporting the ColdFire architecture.

Peripherals Features

The ColdFire V2 Core uses dual 2-stage pipelines to maximize throughput. The Instruction Fetch Pipeline (IFP) and Operand Execution Pipeline (OEP) are decoupled by a FIFO instruction buffer, enabling the IFP to fetch instructions in advance of their use by the OEP, thereby minimizing processor stalls.

Separate clocks for the CPU and system bus enable the ColdFire V2 CPU to operate at a higher frequency than the rest of the system. Local RAM, ROM, and cache, running at the CPU clock rate, further maximize system efficiency by reducing the overall number of system bus accesses, leaving more system bus bandwidth available for other system resources such as other another processor or DMA controller.

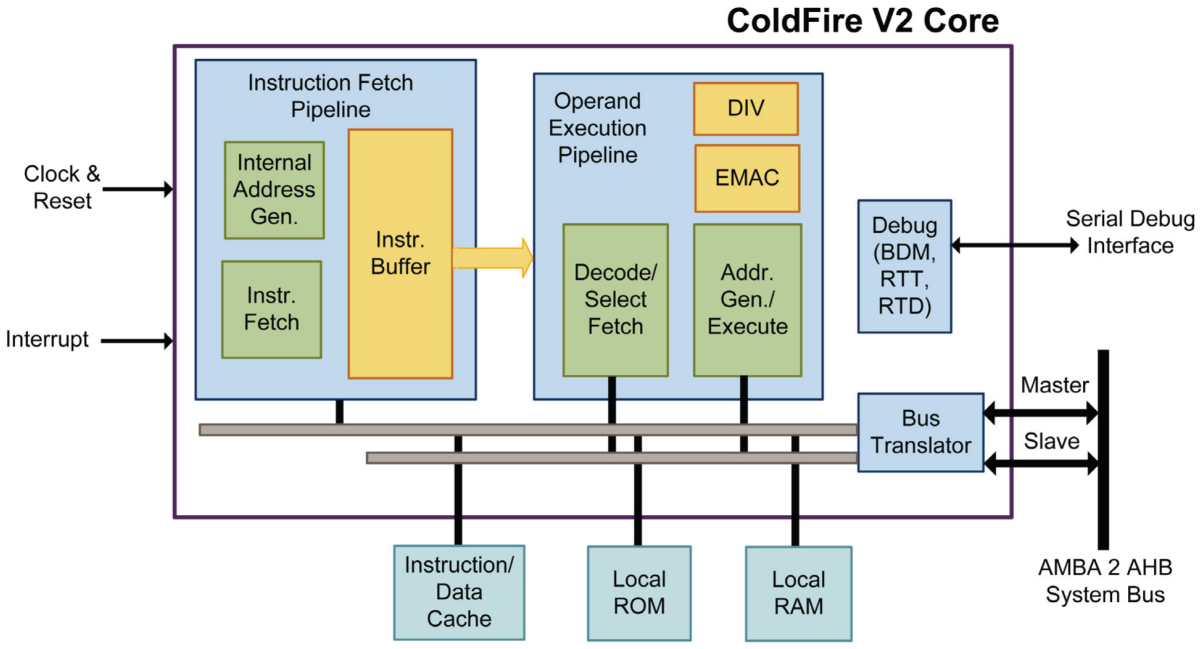
The system bus is the industry standard AMBA 2 AHB. The ColdFire V2 Core includes both an AHB master port and an AHB slave port, which enables an external AHB master to access the ColdFire V2 local RAM.

Applications

Processors based on the ColdFire architecture can be found in over 500 million devices worldwide, powering systems ranging from cameras and printers to robotics and factory automation. ColdFire V2 devices are often used in health care instrumentation, pointof-sale terminals, factory automation, fire and security systems, printers, voice-over-IP stations, and other industrial and consumer applications.

Features

- 32-bit address and data paths
- Variable-length RISC architecture for maximum code density
- ColdFire ISA Revision A+ with dedicated instructions for integrated arithmetic hardware (DIV, EMAC)
- Big-endian data organization
- Up to 32 KB of local RAM with single-cycle access
- Up to 1024 KB of local ROM with single-cycle access



- Up to 32 KB of direct-mapped cache
  - Single-cycle access
  - Configurable as instruction cache, data cache, or split instruction/data cache
- AMBA 2 AHB system bus with master and slave ports DELIVERABLES
  - Master port for ColdFire V2 Core accesses
  - Slave port for external AHB master access to ColdFire V2 local RAM
- Bootable from local RAM, ROM, or system (AHB) memory
- Two-level branch acceleration mechanism for minimum change of- flow execution
- STOP mode for low-power operation
- ColdFire Debug Architecture Revision B+
  - Background Debug Mode (BDM)
  - Real-Time Trace (RTT)
  - Real-Time Debug (RTD)
- Fully synchronous, synthesizable, scannable design

Development Support

The ColdFire architecture, including the ColdFire V2 Core, is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as NXP, Green Hills Software, Wind River Systems, and many more. A free version of the GNU compiler supporting ColdFire V2 targets is also available from www.gnu.org.

NXP offers development boards, software, and CodeWarrior Development Tools (including a free version. In addition, there are several operating systems supporting the ColdFire V2 architecture, including uClinux and several RTOS's, such as the MQX RTOS from Embedded Access, Inc.

Deliverables

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

For more information, please contact us at ip@silvaco.com.

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