ColdFire ® V1 Core

SILVACO

The synthesizable 32-bit RISC ColdFire V1 Core (CFV1CORE) is the smallest and lowest power processor in the ColdFire family, using as few as 19K gates. The CFV1CORE small size and 32-bit performance make it ideal for a wide variety of consumer, healthcare, and other embedded systems applications.

The CFV1CORE provides up to 230 DMIPS of performance at 200 MHz in a typical 90-nm technology. The ColdFire V1 CPU is based on a variable-length RISC architecture that allows instructions to be 16, 32, or 48 bits in length. The result is more efficiently packed code in memory, reducing memory requirements and lowering overall system cost. For DSP operations, the CFV1CORE includes (optional) dedicated hardware multiplier-accumulator (MAC) and divider (DIV) units. Debug support is through a single-wire Background Debug Mode (BDM) interface and includes an on-chip trace buffer.

All ColdFire cores (V1, V2, V3, and V4) share the same architecture and instruction set. Upward compatibility from V1 to V2, V3, and ColdFire V4 processors provides a smooth roadmap to higher performance designs.

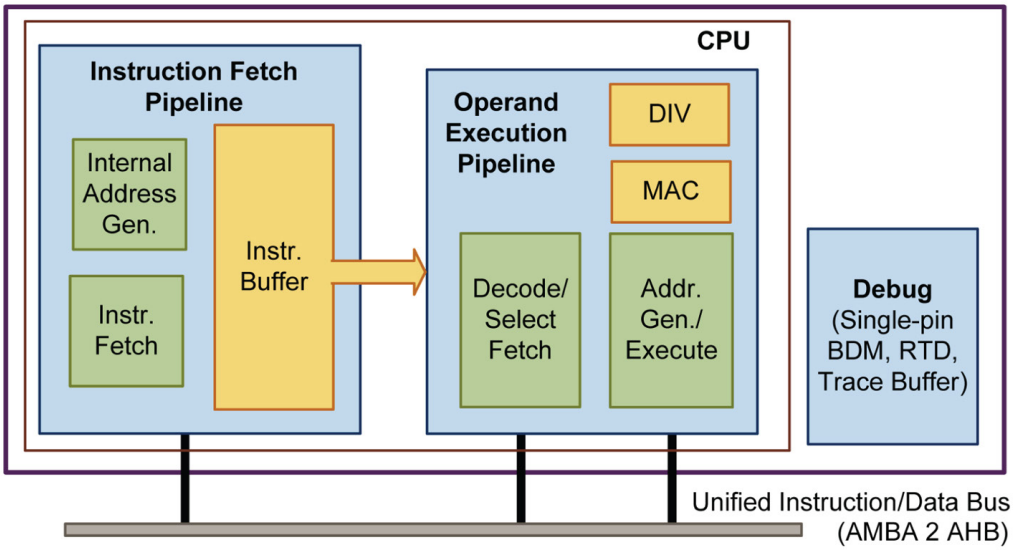
ColdFire architecture has been deployed in over half a billion production devices making it one of the most widely used embedded microprocessors in the world. With the CFV1CORE, you get production-proven processor IP, plus support from the extensive ecosystem of development tools, operating systems, drivers, and libraries supporting the ColdFire architecture.

Features

- 32-bit microprocessor core with 24-bit address bus
- AMBA 2 AHB unified instruction/data bus
- Single-wire debug interface
- Variable-length RISC architecture with 16, 32, and 48-bit instructions
- Independent, decoupled instruction and execution pipelines
- 2-stage Instruction Fetch Pipeline (IFP)
- 2-stage Operand Execution Pipeline (OEP)
- Static branch prediction to minimize change-of-flow execution time
- Execute engines include ALU, barrel shifter, and optional MAC and DIV units
- ColdFire Instruction Set Architecture Rev. C (ISA_C)
- Standard ColdFire programming model with 16 general-purpose, 32-bit registers
- Programmable response upon detection of certain illegal opcodes and illegal addresses (processor exception or system reset)
- Optional debug support including trace and real-time debug (RTD) through a single-wire BDM interface

ColdFire V1 Core

The instruction fetch and execution pipelines are decoupled by an instruction buffer. Instructions can be fetched in advance, thereby minimizing stalls and accelerating throughput.



Debug Support

The optional debug unit provides a rich set of debug capabilities:

- ColdFire Debug B+ functionality mapped into the single-wire BDM interface
- 64x6-bit trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
- Capture of compressed processor status and debug data into trace buffer provides program trace capabilities
- Compression of trace data enables capture of 500-1000 cycles of program trace in 64x6-bit trace buffer
- Real time debug support, with 6 hardware breakpoints (four PC, one address, and one data) that can be configured into a 1 or 2-level trigger with a programmable response (processor halt or interrupt)
- Debug resources are accessible through the single-wire BDM interface or the privileged WDEBUG instruction from the ColdFire V1 CPU
- Debug unit can use the CPU clock (internally divided by 2) or a separate asynchronous clock
- Separate clocks for CPU and debug unit enable shutdown of debug unit when not in use

Ecosystem

The entire ColdFire Family, including the ColdFire V1 Core, is supported by world-class development tools suites offered through leading tools developers including, NXP, Green Hills Software, Wind River Systems and many others. NXP CodeWarrior development tools offer a simple migration path from the Freescale HCS08 to the ColdFire V1 architecture.

Deliverables

The ColdFire V1 Core is delivered in Verilog source code and includes:

- Synthesizable Verilog source code (Source version)
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

The Source version of the CFV1CORE is fully configurable (MAC, DIV, and debug units can be included/excluded through HDL parameter settings).

For more information, please contact us at ip@silvaco.com.

SILVACO
HEADQUARTERS
4701 Patrick Henry Drive, Bldg #23
Santa Clara, CA 95054

NORTH AMERICA sales@silvaco.com
BRAZIL br_sales@silvaco.com
EUROPE eusales@silvaco.com

JAPAN jpsales@silvaco.com
KOREA krsales@silvaco.com
TAIWAN twsales@silvaco.com
SINGAPORE sgsales@silvaco.com
CHINA cn_sales@silvaco.com

WWW.SILVACO.COM

Rev 061920_04
70008