SILVACO

Viso, Belledonne, Brenner

Accelerate Post-layout Parasitics Analysis and Avoid Wasted Simulation Time

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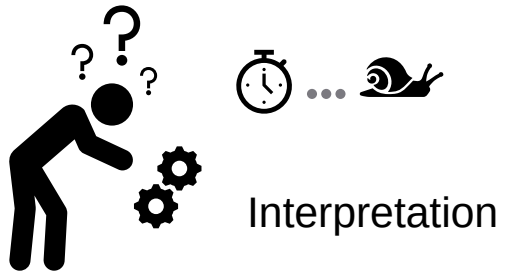
Today's Challenge of Parasitics

- Parasitic elements growing exponentially with advanced nodes
- At 60nm, RC delay from interconnects is already more important than gate delay
- Interconnects and layout parasitics black-boxes now creating significant problems
- Timing, distortion, cross-coupling, noise, IR drop, EM, ESD, etc.

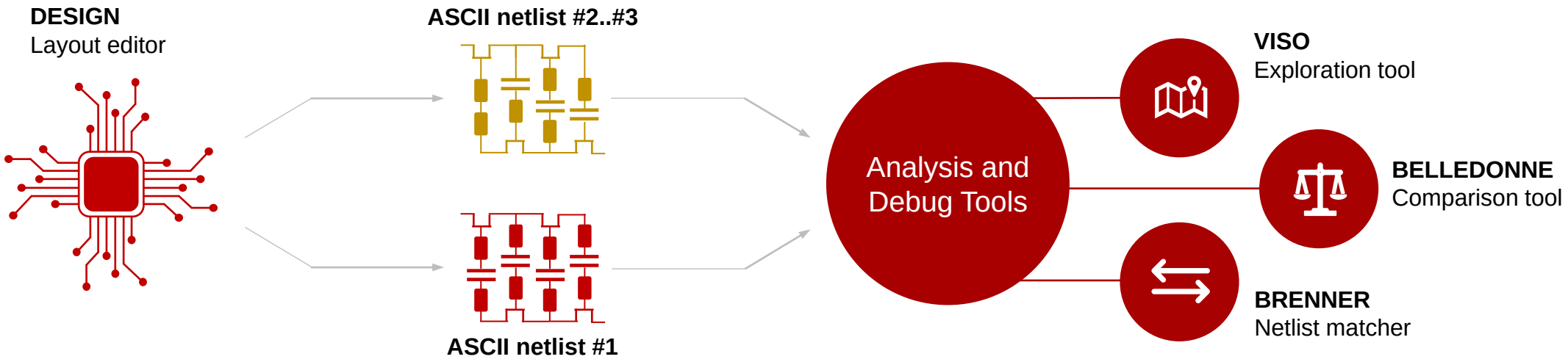
Today's Challenge of Parasitics

- To counter the impact of the parasitics on project schedules, a possible solution is to improve the simulation runtime
- There is a constant race to deliver the fastest simulator from different EDA vendors
- However, the interpretation of the simulation results and its complexity is underestimated
- Parasitics effect in advanced technologies leads to an overall rethink of the design flow, its optimization and its debug which takes way longer than a simulation.



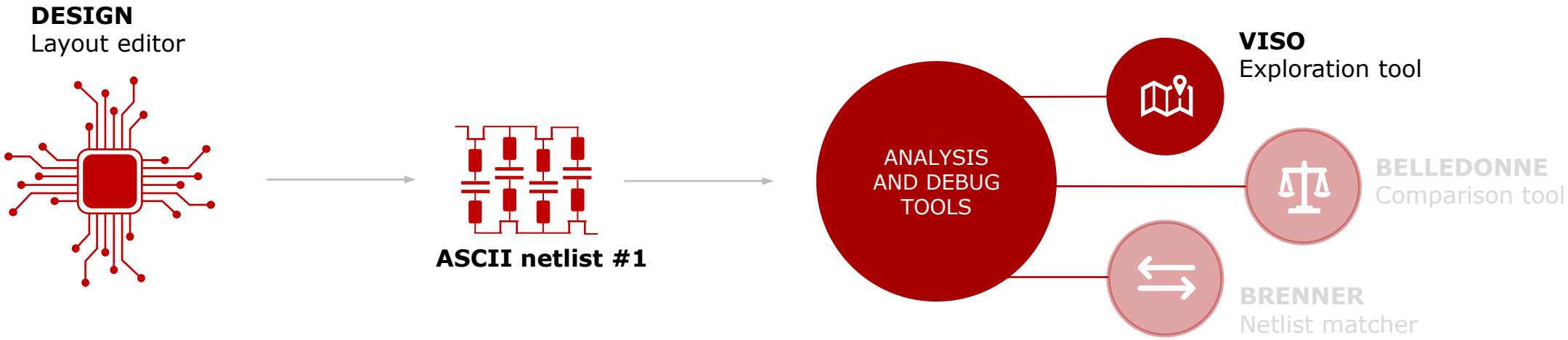
Today's Challenge of Parasitics

- Silvaco has developed tools that ease parasitic extraction flow setup, save simulation time and enable powerful physical design debug
  - BRENNER: netlist matcher
  - BELLEDONNE: comparison tool
  - VISO: exploration tool



Viso
Parasitics Analysis and Exploration

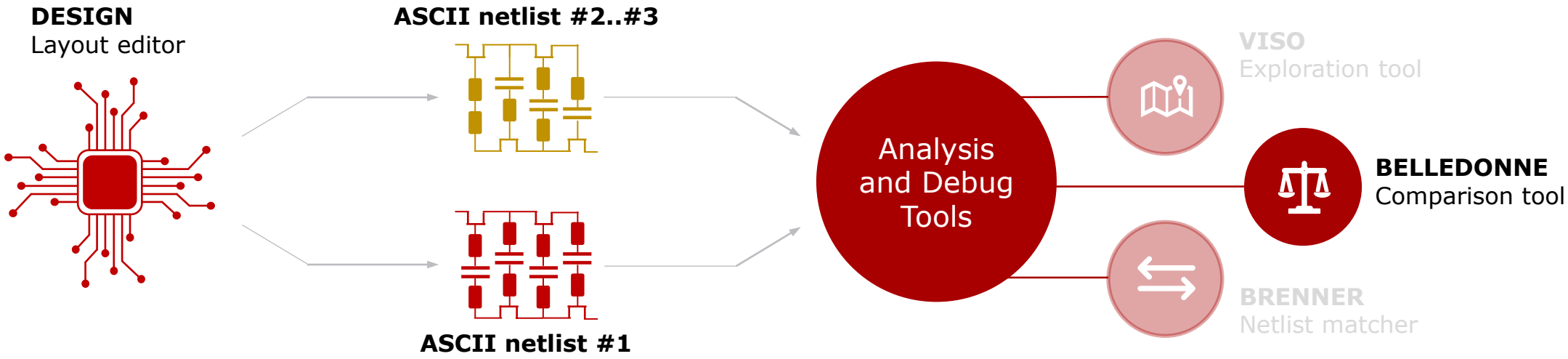
- VISO: analysis and exploration of parasitics
  - All interconnect related problems
  - Key parameters: resistance, capacitance, RC delay
  - Detailed analysis, smart tabular views
  - Graphics with 2D and 3D view, batch mode



Belledonne

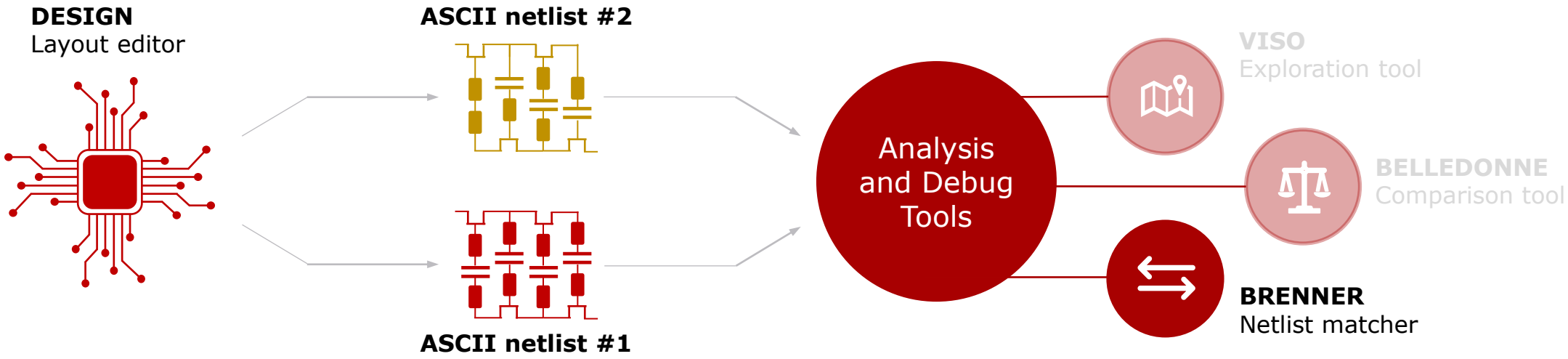
Comparison of Extracted Netlists with Parasitics

- BELLEDONNE: comparison of extracted netlists with parasitics
  - Comparison of two or more extracted netlists
  - Input: any extracted netlists of similar layout
  - Compares statistics, P2P resistances and RC delays, NET to NET capacitances
  - Batch mode and graphical user interface



Brenner
Netlist Matcher

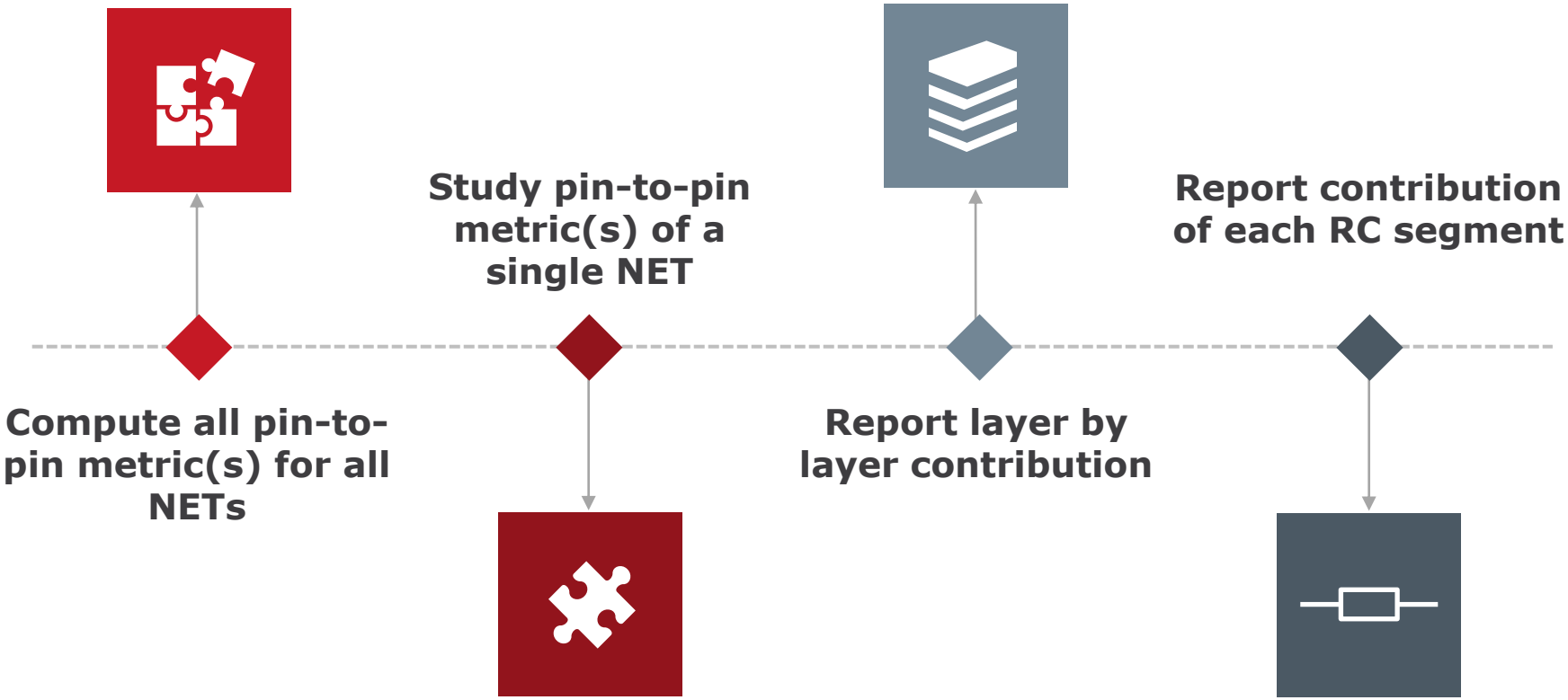
- BRENNER: netlist matcher
  - Matching of two different netlists at finger level
  - Matches instances, pins, NETs. Comparison of devices parameters.
  - Often used in conjunction with BELLEDONNE. Mandatory if corresponding NET and pin names do not match



Viso and Belledonne

Parasitics Analysis and Abstraction

- VISO and BELLEDONNE analyses enable different levels of abstraction
  - From compiled results for a given metric to a very detailed level



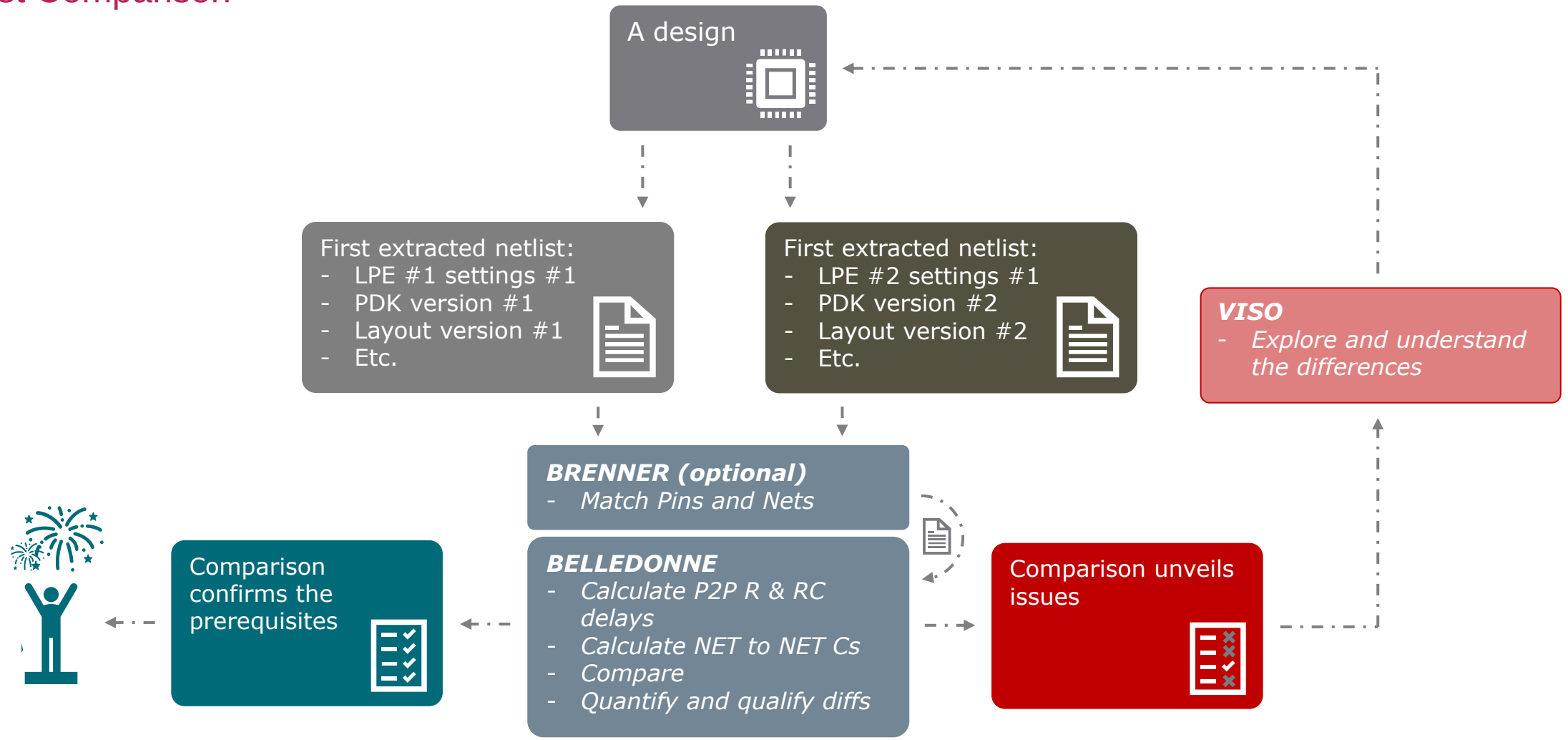
Viso and Belledonne
Flexibility

- VISO and BELLEDONNE offer flexibility through three different flows

- Graphical User Interface (GUI)
  - Allows to access to all the options
  - Powerful to debug and inspect results
- Command line
  - Support most of commands / options
  - Powerful to trigger batch runs
- XML file
  - Support all commands / options
  - Can be scripted to trigger batch runs

Brenner and Belledonne

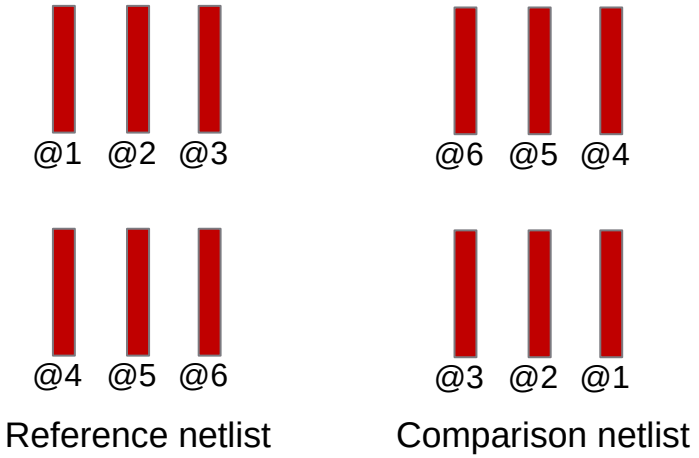
Netlist Comparison



Brenner and Belledonne
Netlist Comparison

- BELLEDONNE relies on NET and pin names to compare data
  - When NETs or pins name does not match, one need to use BRENNER

- Typical cases where BRENNER needs to be used first:
  - Different strategies for NET and pin naming:
    - F1250 vs net72_2
    - XM1:src vs XM1:s
  - Different delimiters
    - ":" vs "#"
  - Fingers scrambling

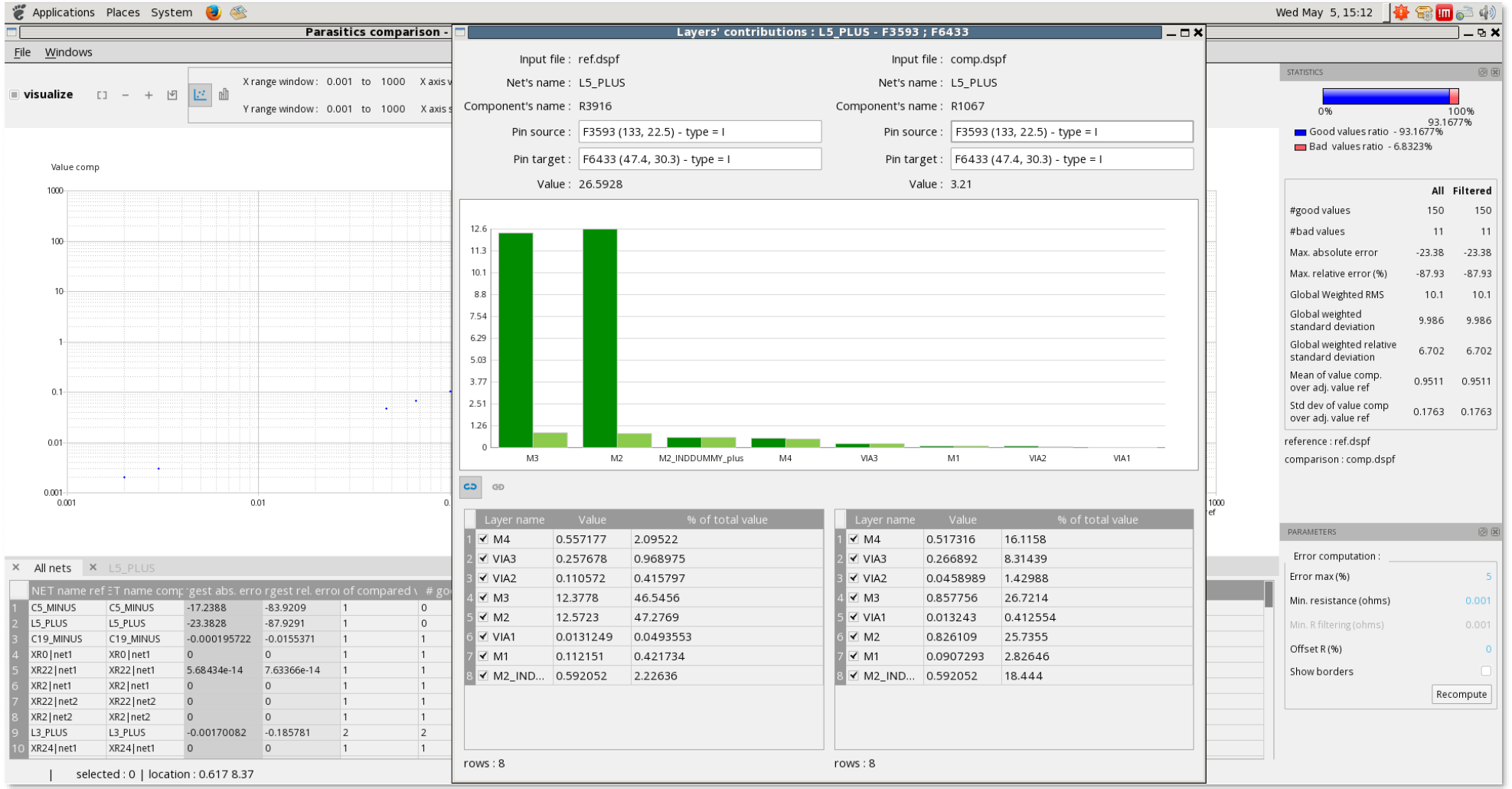


Brenner and Belledonne
Netlist Comparison

- BELLEDONNE combines two capabilities
  - Computation of parasitics related metrics
    - Number of pins / NETs / Rs / Cs / etc. (statistics)
    - Pin to pin Rs
    - Pin to pin RC delays
    - NET to NET Cs
- Report of differences
  - Qualify and quantify the differences
  - Display the differences using the GUI with a possibility to continue the exploration into VISO

- BELLEDONNE for end users
  - Extraction QA
  - Any kind of comparison

Brenner and Belledonne
Netlist Comparison



Viso
Explore and Analyze

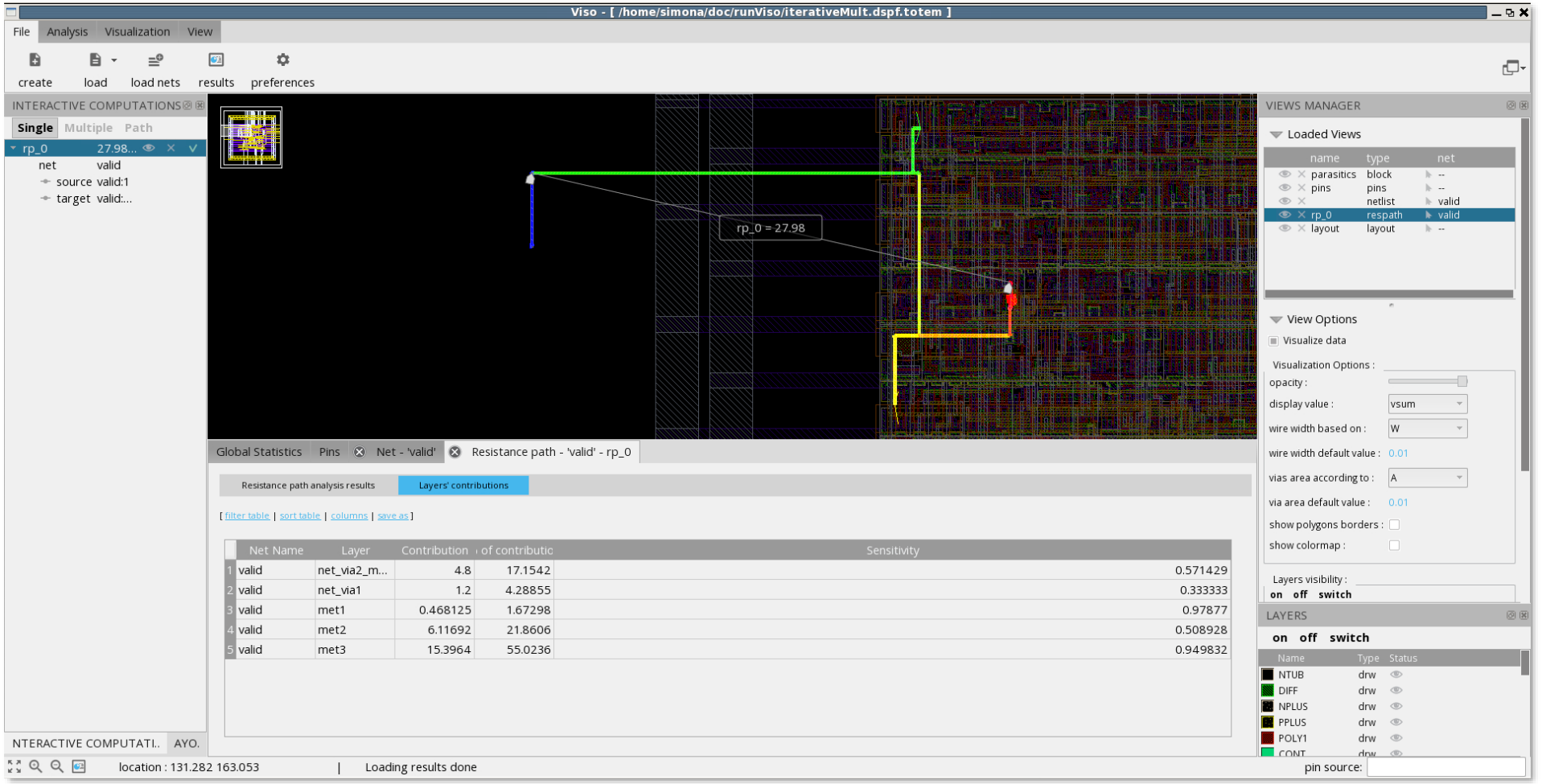
- VISO provides analyses for a deep understanding and debug of the designs combined with a powerful GUI for the visualization
  - Parasitic related analysis
    - Node to node Rs and RC delay; resistance and RC delay path
    - NET to NET Cs
    - Comparison of NETs (buses, differential pair, etc.)
    - Static IR drop
    - Grid resistance / delay distribution
    - Detection of cut NETs, sanity checks
  - Exploration through the GUI
    - 2D and 3D view with the GDSII on top of the parasitics
    - Interpretation of results simplified through graphics
    - Ease of use

Viso
Explore and Analyze

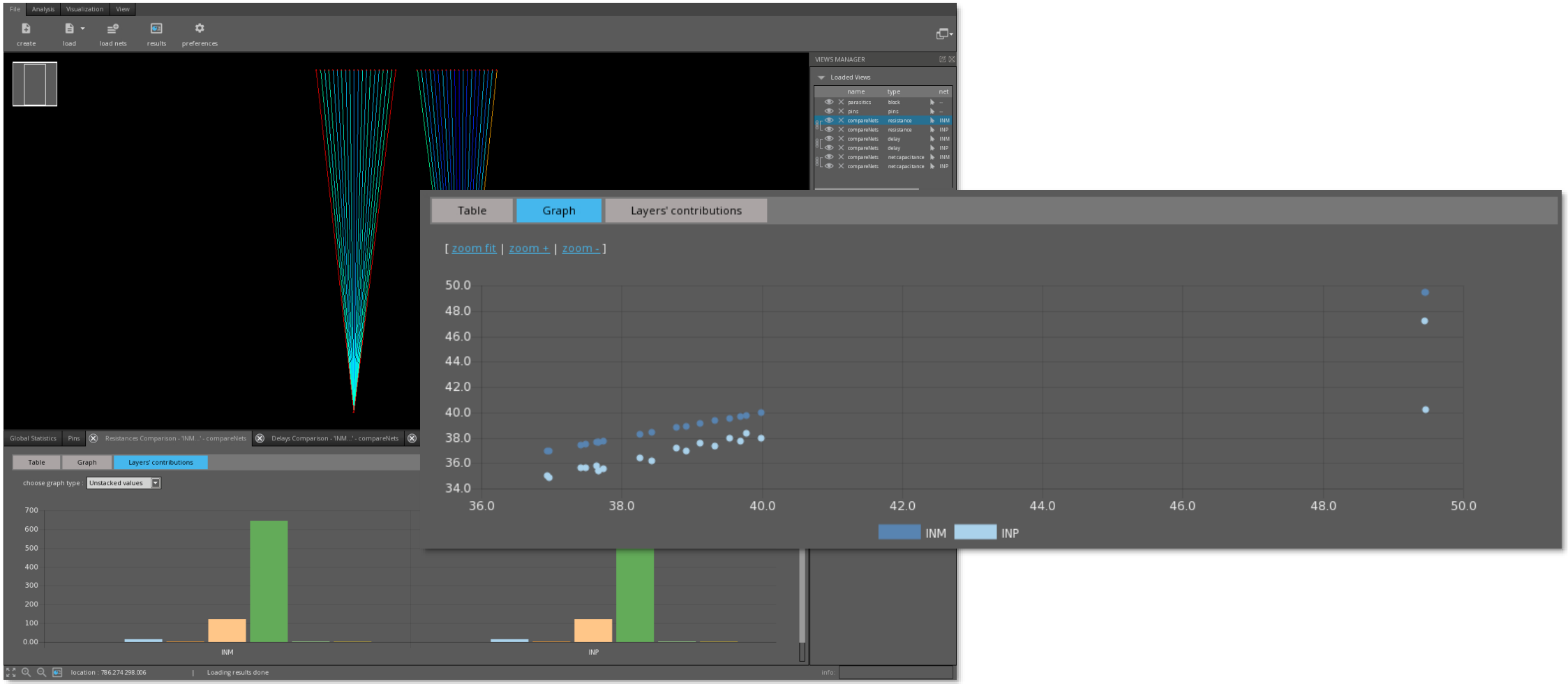
- VISO for end users
  - Verify balance of R, RC delays and NET to NET C
    - Delay skew checker
    - Diff pair matching control
  - Extraction QA
    - Debug
    - Sanity checks
  - EM/IR quick analyzer
  - Parasitic explorer
  - Build up customized analysis flows

- VISO helps designers to solve parasitic issues without having to rely on costly simulation

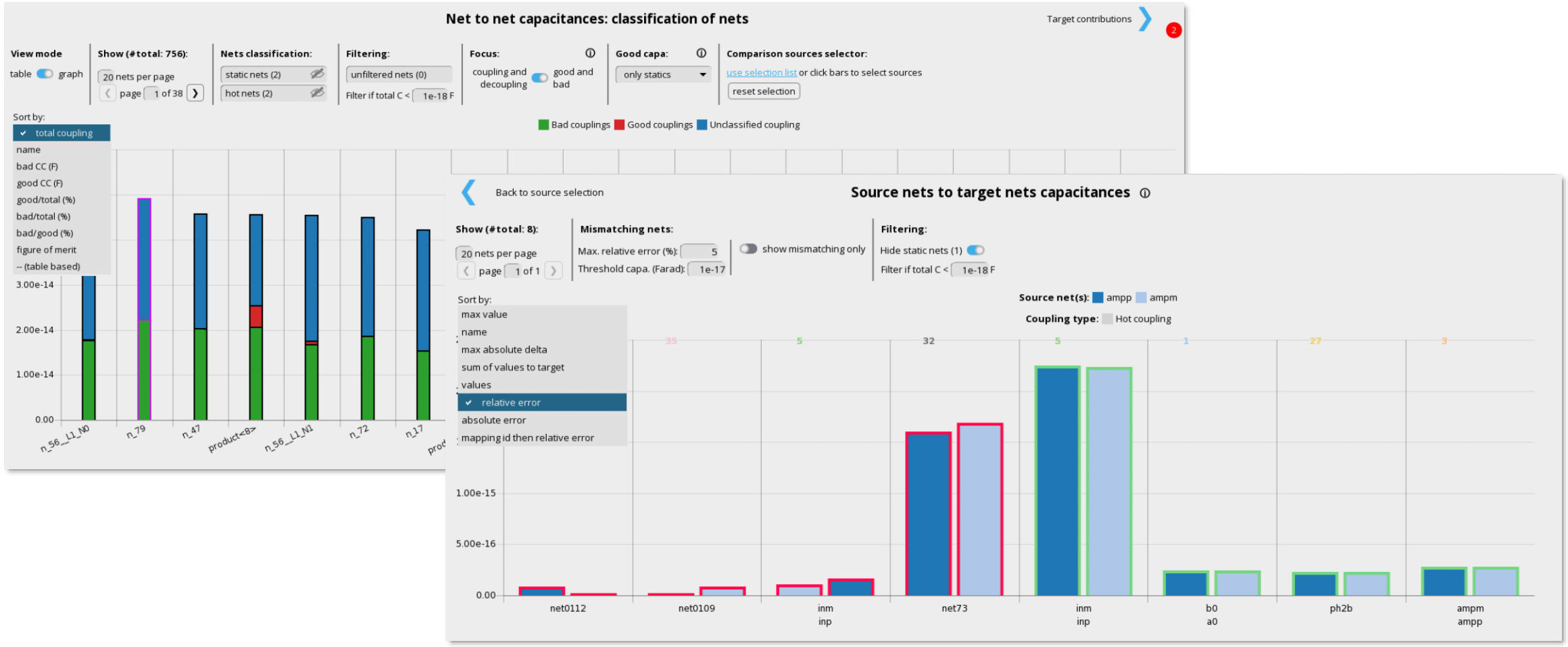
Viso
Explore and Analyze



Viso
Explore and Analyze



Viso
Explore and Analyze



Viso, Belledonne, Brenner

Summary

- Simulations become less relevant when the results cannot be interpreted correctly
- Additional solutions are now a must have to provide insight when diving in the parasitics black-box

- BRENNER, BELLEDONNE and VISO powerful capabilities combined with the user knowledges offer countless possibilities
  - Build an extraction QA methodology
  - Pre-simulation debugging of the design
  - Critical path optimization