SILVACO

Victory RCx Pro Physics-Based Parasitic Extraction

User Guide

Introduction

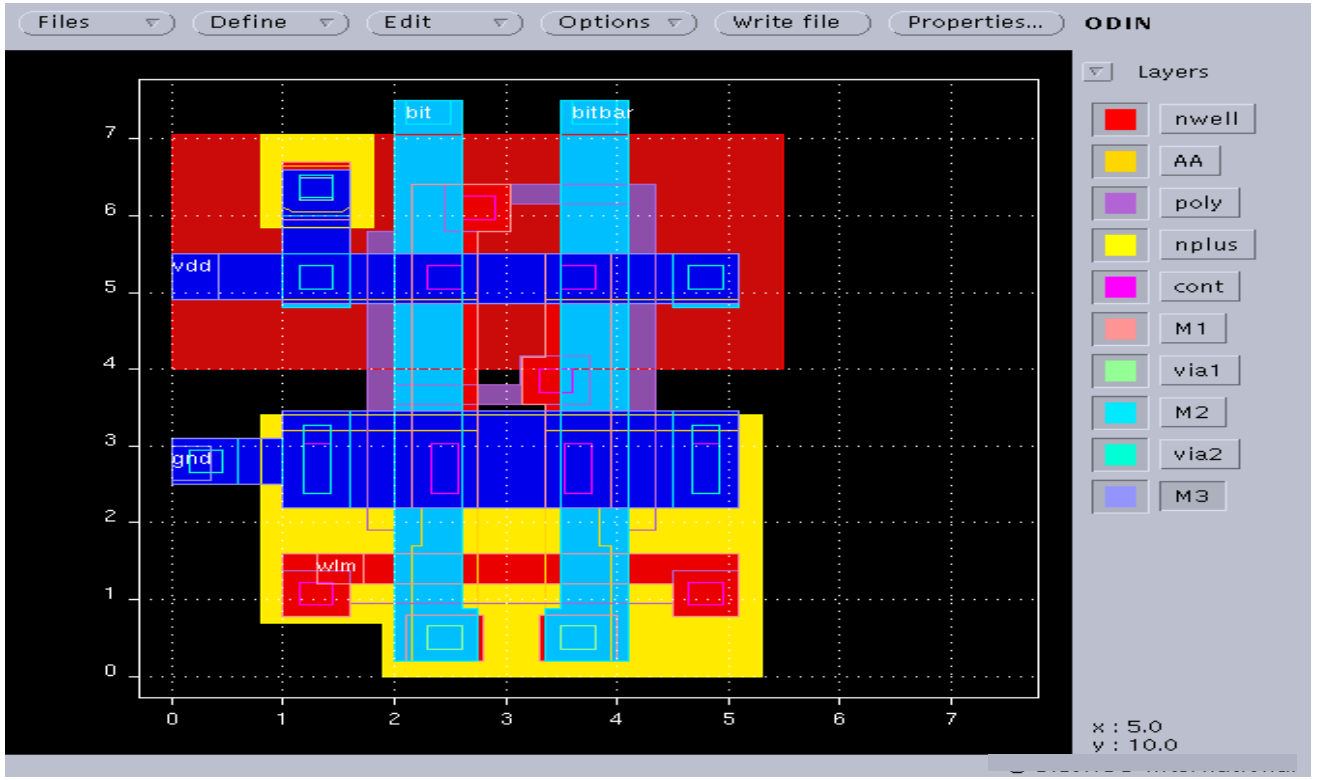
- This workshop will show how to use Victory RCx Pro using an SRAM example
- Areas covered:
  - INPUT (External Information)
    - Mask Layouts
    - Process Flow
  - INPUT (User Generated)
    - Creating a MAP File
    - Creating an Input File
  - OUTPUT information
    - Cell Parasitic Netlist
    - 3D Structure File
- Conclusions

Input

- Input information:
  - 1/ Mask Layouts (GDS2 or Silvaco's MaskViews format)
  - 2/ Process Flow

Masks

- The original mask layout:



MAP File

- This mask is then modified by the map file in the input deck:
- The map file consists of 4 operations:
  - 1/ Various regions of the active devices are defined by logical combinations of the original mask
  - 2/ The user has the option to export any of the newly created logical mask combinations to the layout in MaskViews for viewing and debugging
  - 3/ The connectivity of the cell is defined
  - 4/ The active device terminals are defined

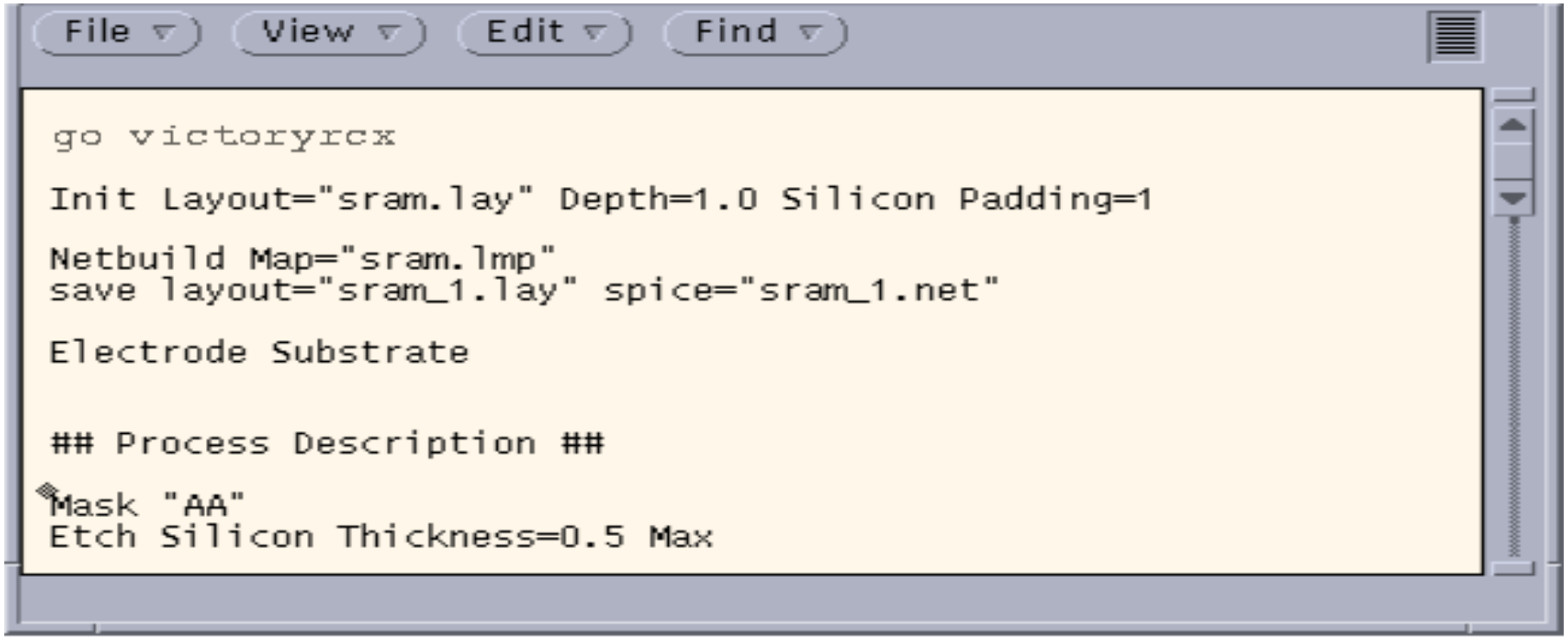
Map File

File View Edit Find

```
AND !nwell AA NACTIVE
AND nwell AA PACTIVE
AND NACTIVE poly NGATE
AND PACTIVE poly PGATE
AND NACTIVE !poly NSD1
AND PACTIVE !poly PSD1
AND NSD1    nplus NSD
AND PSD1   !nplus PSD
NOT !nwell  NSD NSUB
NOT  nwell  PSD PSUB
NOT cont poly SICONT
NOT cont poly SCONT

; Export new masks

export SICONT
export NSD
export NSUB
export PSD
export PSUB
export SCONT

; Define connectivity

Connect SICONT cont
Connect poly cont
Connect cont M1
Connect M1 via1
Connect via1 M2
Connect M2 via2
Connect via2 M3
Connect NGATE poly
Connect NSD cont
Connect PGATE poly
Connect PSD cont
Connect NSUB SCONT
Connect PSUB SCONT
Connect cont SCONT

; Define device name, gate, source/drain, substrate and connection

ELEMENT MOS[myNMOS]  NGATE   NSD    NSUB   SICONT
ELEMENT MOS[myPMOS]  PGATE   PSD    PSUB   SICONT
```

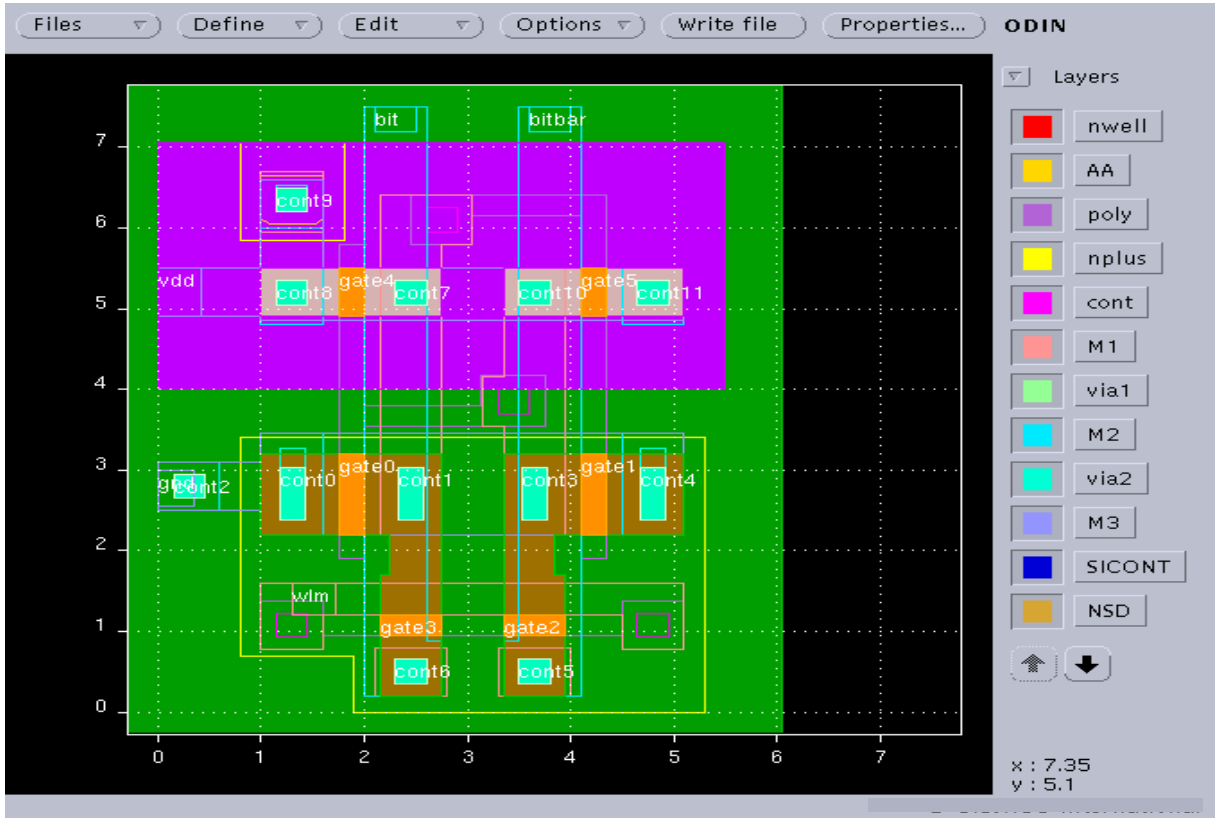
INPUT File

- Initialization and Mask Annotation



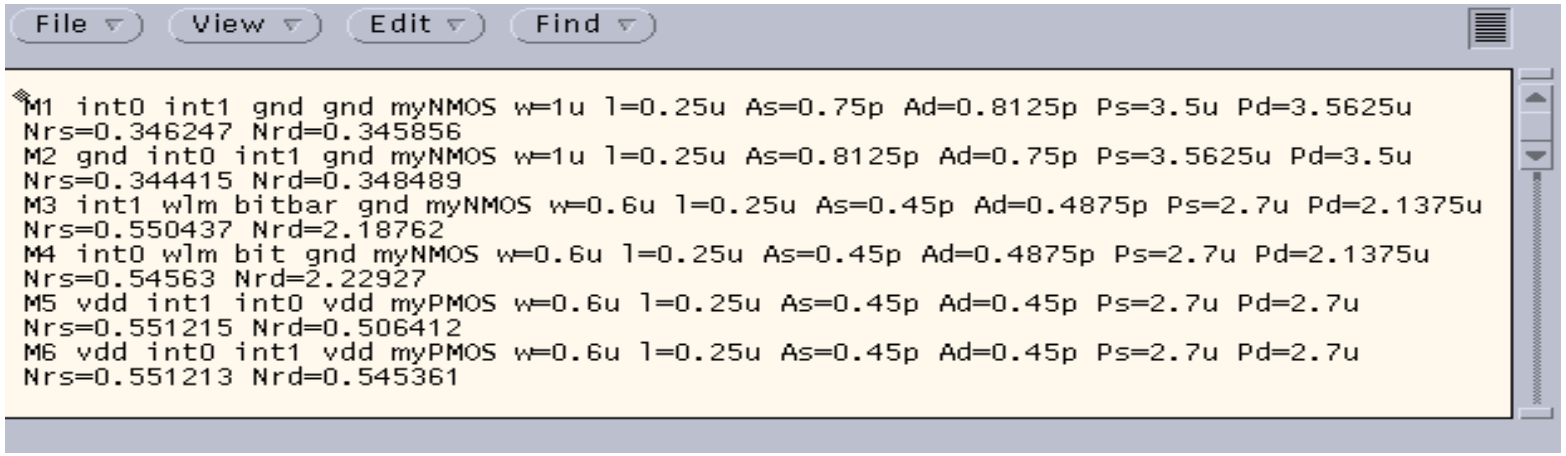
Annotated/Modified Map File

- Victory RCx will generate the new masks and annotate electrodes etc from the map file



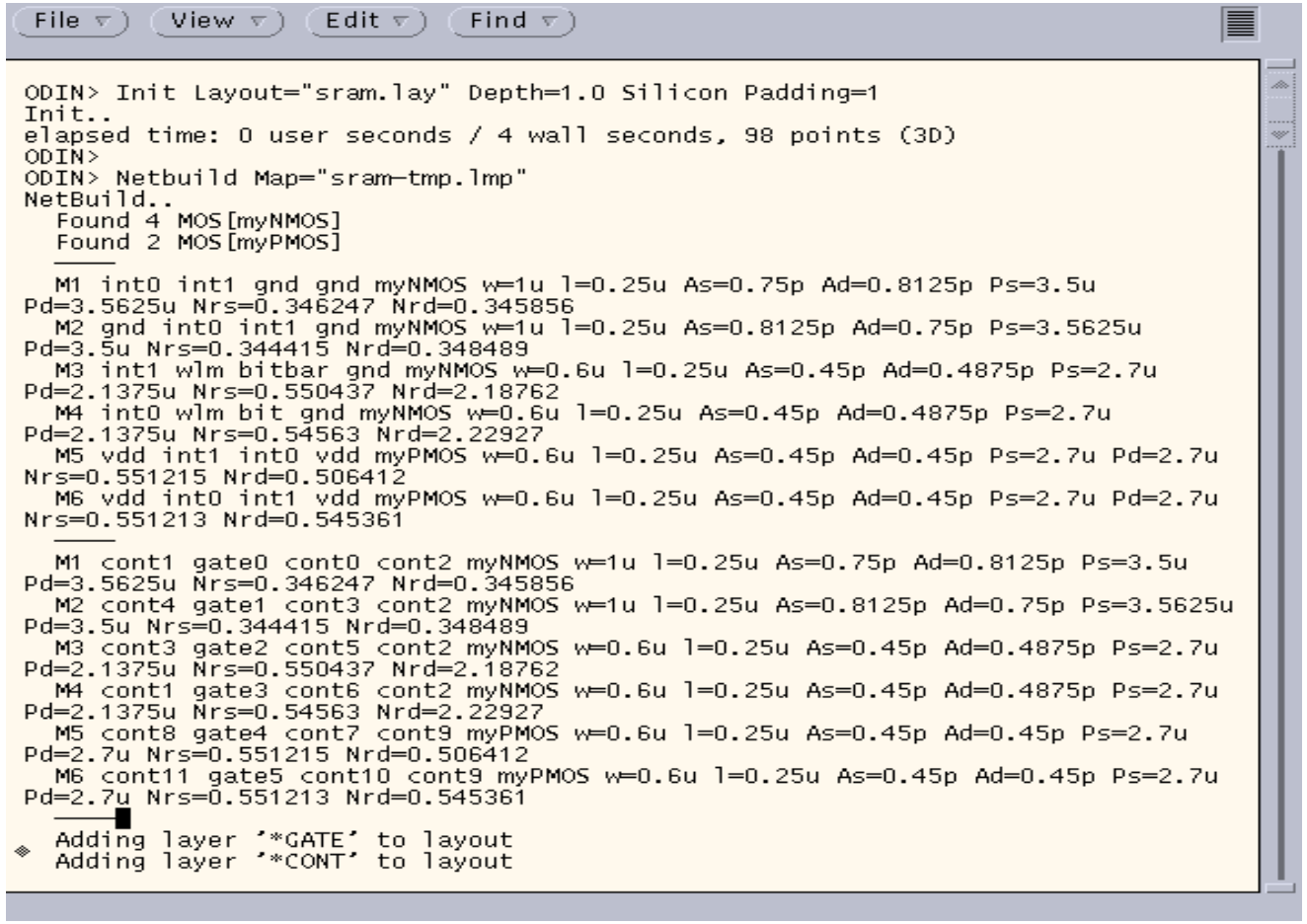
Device Net List

- A device net list can be exported to a text file for debugging



Device Net List

- When the program is run, two net lists are printed in the runtime output for debugging



INPUT File

File View Edit Find

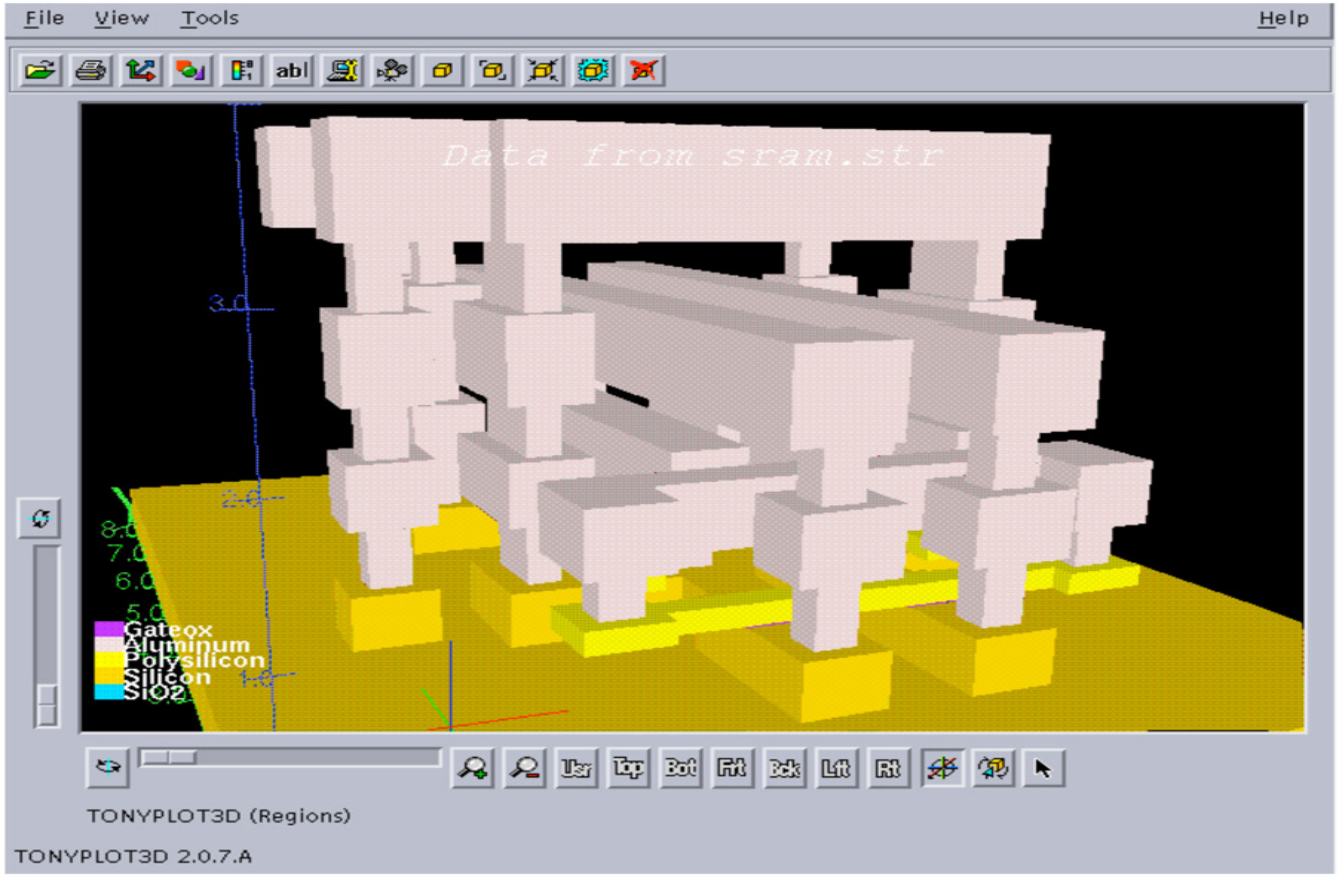
```
go victoryrox simsflags="-V 1.0.6.A"

Init Layout="sram.lay" Depth=1.0 Silicon Padding=1

Netbuild Map="sram.lmp"
save layout="sram_1.lay" spice='sram_1.net'

Electrode Substrate


## Process Description ##

Mask "AA"
Etch Silicon Thickness=0.5 Max
Strip Resist

Deposit Oxide Thickness=0.0 Max

Deposit Material('Gateox') Thickness=0.01 Max
Mask "*GATE" reverse
Etch Material('Gateox')
Strip Resist

Deposit Oxide Thickness=0.0 Max

Deposit Poly Thickness=0.2 Max
Mask "poly"
Etch Poly
Strip resist

Electrodes "*GATE" Poly

# Contact
Deposit Oxide Thickness=0.4 Max

Mask "cont" Reverse
Etch Oxide
Strip Resist

# Stop Source/Drain/Substrate Contacts Shorting to Substrate
Deposit Oxide Thickness=0.01 Min
Electrodes "*CONT" Oxide
# Named polygons will be converted into electrodes
```

INPUT File

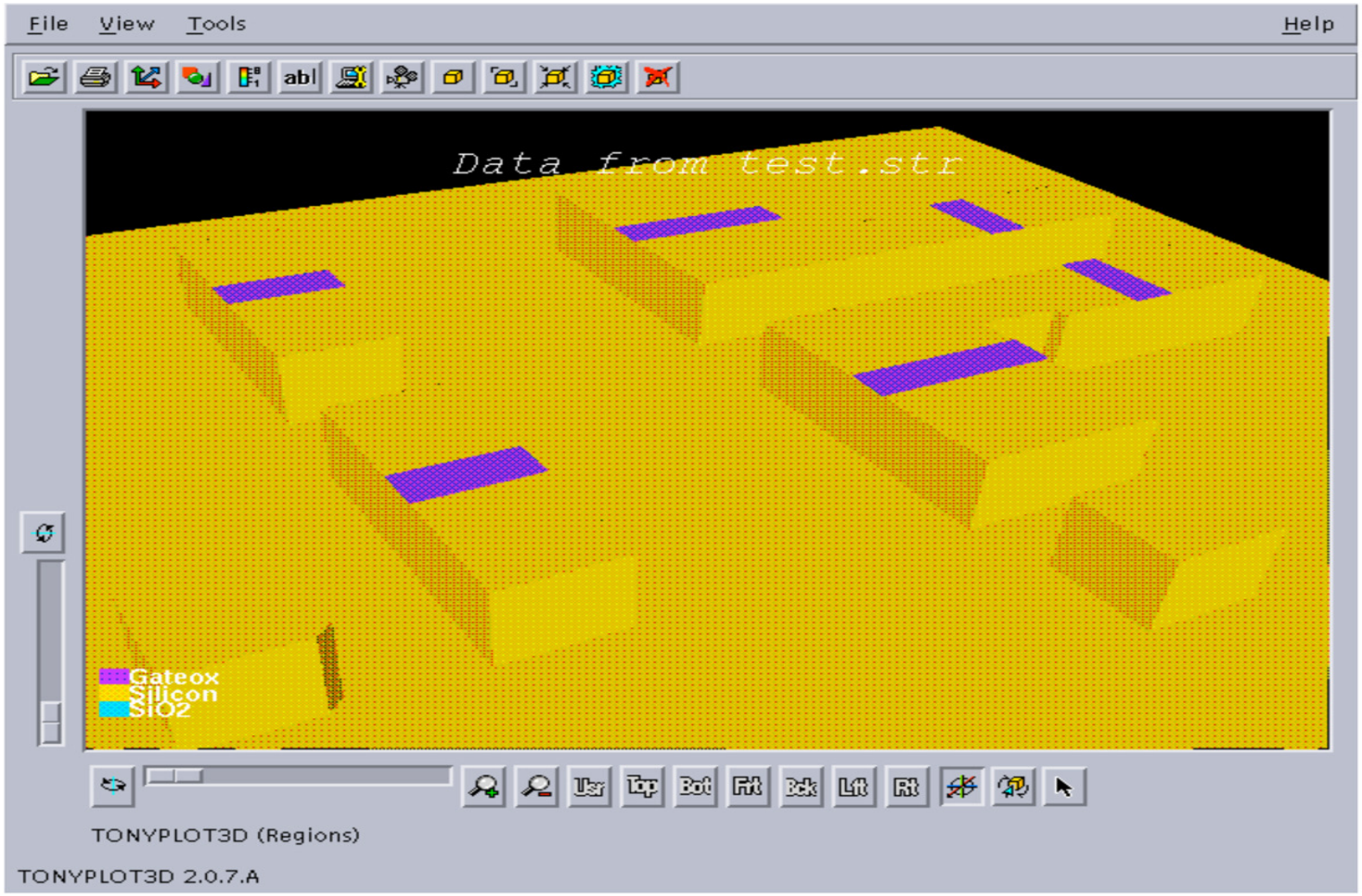
File View Edit Find

```
# Metal 1
Deposit Aluminum Thickness=0.6 Max
Mask "M1"
Etch Aluminum
Strip resist
Electrodes "M1" Aluminum

# M1/M2 via
Deposit Oxide Thickness=0.5 Max

Mask "via1" Reverse
Etch Oxide
Strip Resist

# M2
Deposit Aluminum Thickness=0.8 Max
Mask "M2"
Etch Aluminum
Strip Resist
Electrodes "M2" aluminum

# M1/M2 via
Deposit Oxide Thickness=0.6 Max

Mask "via2" Reverse
Etch Oxide
Strip Resist

# M3
Deposit Aluminum Thickness=1.0 max

Mask "M3"
Etch Aluminum
Strip Resist
Electrodes "M3" aluminum

deposit oxide thickness=1.0 max

save structure="sram.str"

material Silicon Conductivity=1
material material("Gateox") Perm=0.01

Interconnect resistance adapt=0.05
Interconnect capacitance adapt=0.05
```

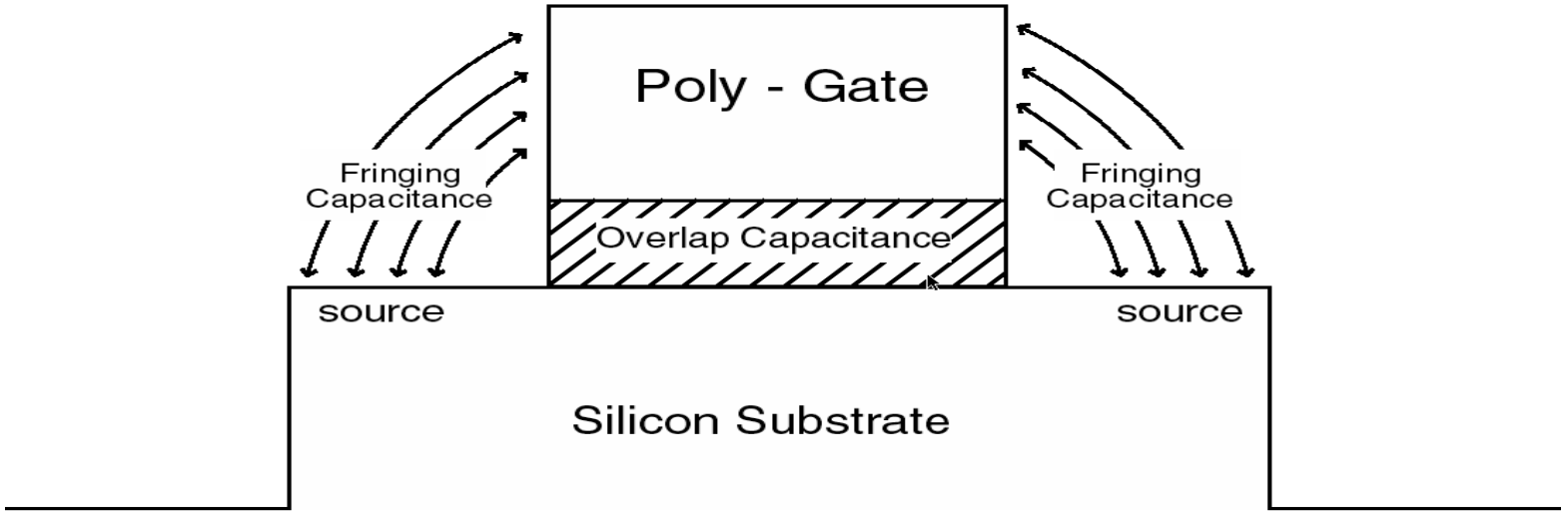
3D-Structure File



3D-Structure File



Gate Fringing Capacitance



Extrinsic Capacitance: Fringing Capacitance

- The fringing capacitance consists of bias independent outer fringing capacitance
- The outer fringing capacitance can be theoretically calculated:

$$CF = \frac{\varepsilon_{ox}}{\alpha} \, In\left(1 + \frac{t_{poly}}{t_{ox}}\right) \qquad \alpha = \frac{\pi}{2}$$

Parasitic Netlist

- Connectivity and Resistance...

File View Edit Find

```
M1 cont1 gate0 cont0 cont2 myNMOS w=1u l=0.25u As=0.75p Ad=0.8125p Ps=3.5u
Pd=3.5625u Nrs=0.346247 Nrd=0.345856
M2 cont4 gate1 cont3 cont2 myNMOS w=1u l=0.25u As=0.8125p Ad=0.75p Ps=3.5625u
Pd=3.5u Nrs=0.344415 Nrd=0.348489
M3 cont3 gate2 cont5 cont2 myNMOS w=0.6u l=0.25u As=0.45p Ad=0.4875p Ps=2.7u
Pd=2.1375u Nrs=0.550437 Nrd=2.18762
M4 cont1 gate3 cont6 cont2 myNMOS w=0.6u l=0.25u As=0.45p Ad=0.4875p Ps=2.7u
Pd=2.1375u Nrs=0.54563 Nrd=2.22927
M5 cont8 gate4 cont7 cont9 myPMOS w=0.6u l=0.25u As=0.45p Ad=0.45p Ps=2.7u
Pd=2.7u Nrs=0.551215 Nrd=0.506412
M6 cont11 gate5 cont10 cont9 myPMOS w=0.6u l=0.25u As=0.45p Ad=0.45p Ps=2.7u
Pd=2.7u Nrs=0.551213 Nrd=0.545361
R1 aux1 gate5 0.00137841
R2 aux1 gate1 0.960747
R3 aux1 aux2 1.24795
R4 aux2 cont7 0.183696
R5 aux2 cont1 0.277647
R6 aux3 cont10 0.285937
R7 aux3 aux4 0.816721
R8 aux3 cont3 0.170574
R9 aux4 gate0 0.24963
R10 aux4 gate4 0.658176
R11 gate3 aux5 0.119968
R12 gate2 aux5 0.187146
R13 aux5 wlm 0.284485
R14 cont6 bit 0.761713
R15 cont5 bitbar 0.744059
R16 aux7 cont2 0.619897
R17 aux7 cont0 0.302136
R18 aux7 gnd 0.0392137
R19 aux7 cont4 0.373016
R20 aux9 vdd 0.0549862
R21 aux9 cont8 0.627792
R22 aux9 cont11 0.73004
R23 aux9 cont9 0.639424
C1 cont0 cont1 1.73977e-18
C2 cont0 gate0 1.75647e-18
C3 cont0 cont3 1.75647e-18
C4 cont0 gate1 1.73977e-18
C5 cont0 cont5 2.49126e-17
C6 cont0 gate2 3.52452e-18
C7 cont0 bitbar 2.49126e-17
C8 cont0 wlm 3.52452e-18
C9 cont0 cont6 2.51231e-17
C10 cont0 gate3 3.52452e-18
```

Parasitic Netlist

File View Edit Find

```
C1 cont0 cont1 1.73977e-18
C2 cont0 gate0 1.75647e-18
C3 cont0 cont3 1.75647e-18
C4 cont0 gate1 1.73977e-18
C5 cont0 cont5 2.49126e-17
C6 cont0 gate2 3.52452e-18
C7 cont0 bitbar 2.49126e-17
C8 cont0 wlm 3.52452e-18
C9 cont0 cont6 2.51231e-17
C10 cont0 gate3 3.52452e-18
C11 cont0 bit 2.51231e-17
C12 cont0 cont7 1.73977e-18
C13 cont0 cont8 5.56597e-18
C14 cont0 gate4 1.75647e-18
C15 cont0 cont9 5.56597e-18
C16 cont0 vdd 5.56597e-18
C17 cont0 cont10 1.75647e-18
C18 cont0 cont11 5.56597e-18
C19 cont0 gate5 1.73977e-18
C20 cont0 aux1 5.2193e-18
C21 cont0 aux2 5.2193e-18
C22 cont0 aux3 5.2694e-18
C23 cont0 aux4 5.2694e-18
C24 cont0 aux5 1.05736e-17
C25 cont0 aux9 2.22639e-17
C26 cont0 substrate 2.93852e-16
C27 cont1 gate0 5.25491e-18
C28 cont2 cont1 1.73977e-18
C29 gnd cont1 1.73977e-18
C30 cont1 cont3 5.25491e-18
C31 cont4 cont1 1.73977e-18
C32 cont1 cont5 3.41577e-18
C33 cont1 gate2 1.05122e-18
C34 cont1 bitbar 3.41577e-18
C35 cont1 wlm 1.05122e-18
C36 cont1 cont6 1.32857e-17
C37 cont1 gate3 1.05122e-18
C38 cont1 bit 1.32857e-17
C39 cont1 cont8 2.10034e-18
C40 cont1 gate4 5.25491e-18
C41 cont1 cont9 2.10034e-18
C42 cont1 vdd 2.10034e-18
C43 cont1 cont10 5.25491e-18
C44 cont1 cont11 2.10034e-18
C45 cont1 aux3 1.57647e-17
C46 cont1 aux4 1.57647e-17
C47 cont1 aux5 3.15367e-18
C48 aux7 cont1 6.95907e-18
C49 cont1 aux9 8.40134e-18
C50 cont1 substrate 2.3348e-16
C51 cont2 gate0 1.75647e-18
C52 gnd gate0 1.75647e-18
C53 cont4 gate0 1.75647e-18
C54 gate1 gate0 5.25491e-18
C55 gate0 cont5 1.04764e-17
C56 gate0 gate2 1.03393e-18
C57 gate0 bitbar 1.04764e-17
C58 gate0 wlm 1.03393e-18
C59 gate0 cont6 1.35793e-18
C60 gate0 gate3 1.03393e-18
C61 gate0 bit 1.35793e-18
C62 cont7 gate0 5.25491e-18
C63 gate0 cont8 1.32368e-18
C64 gate0 cont9 1.32368e-18
C65 gate0 vdd 1.32368e-18
C66 gate0 cont11 1.32368e-18
C67 gate5 gate0 5.25491e-18
C68 aux1 gate0 1.57647e-17
C69 aux2 gate0 1.57647e-17
C70 gate0 aux5 3.10179e-18
C71 aux7 gate0 7.02587e-18
```

Realistic Processing

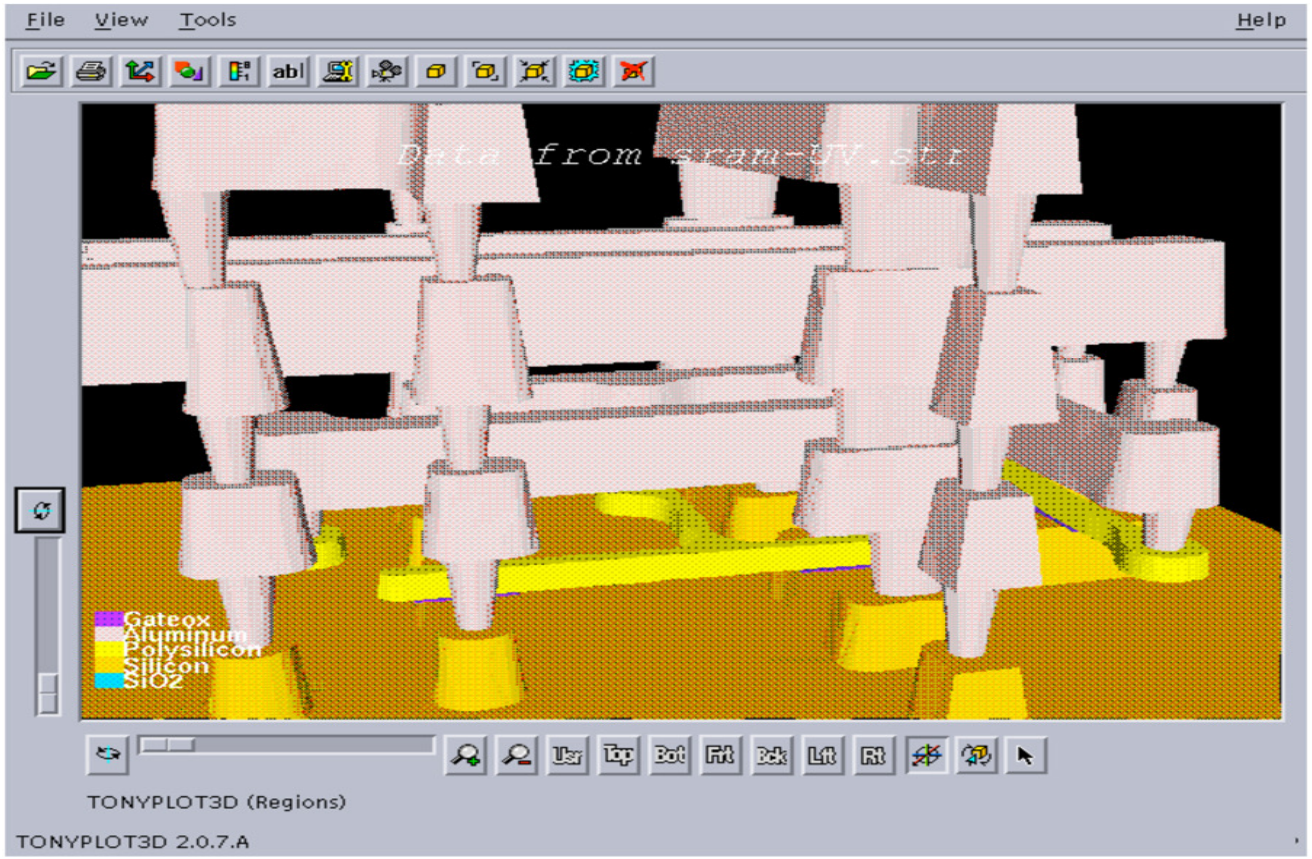
- Input deck...

File View Edit Find

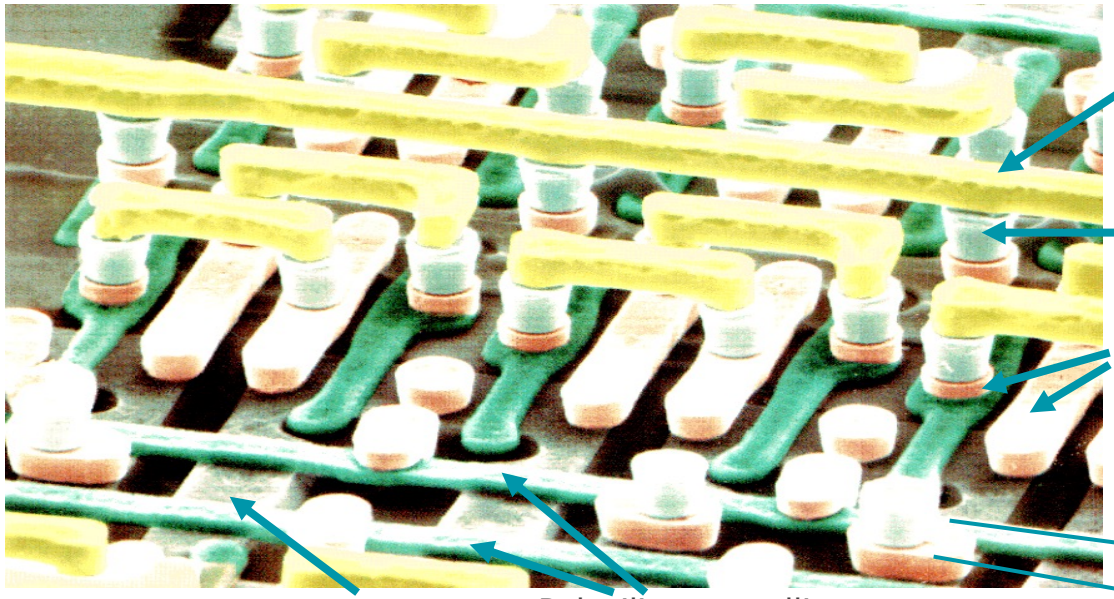
```
go victoryroa simsflags='-V 1.0.7.A'

Init Layout='sram.lay" Depth=1.0 Silicon Padding=1

Netbuild Map="sram.lmp"
save layout='sram_1.lay' spice="sram_1.net"

Electrode Substrate


## Process Description ##

Illumination Wavelength=DUVLINE

Deposit Resist Thickness=0.1 Max
Mask 'AA" Litho CriticalIntensity=0.5 Aperture=0.5 Defocus=0
Etch Silicon Rate=1 Time=0.5 Isotropic=0.1
Strip Resist

Deposit Oxide Thickness=0.0 Max

Deposit Material('Gateox') Thickness=0.01 Max
Mask '*GATE' reverse
Etch Material("Gateox")
Strip Resist

Deposit Oxide Thickness=0.0 Max

Deposit Poly Thickness=0.2 Max
Deposit Resist Thickness=0.1 Max
Mask 'poly" Litho CriticalIntensity=0.5 Aperture=0.5 Defocus=0
Etch Poly Rate=1 Time=0.22 Isotropic=0.1
Strip resist

Electrodes '*GATE' Poly

# Contact
Deposit Oxide Thickness=0.4 Max
Mask 'cont" Litho CriticalIntensity=0.5 Aperture=0.5 Defocus=0 Reverse
Etch Oxide Rate=1 Time=0.55 Isotropic=0.1
Strip Resist

# Stop Source/Drain/Substrate Contacts Shorting to Substrate
Deposit Oxide Thickness=0.01 Min
Electrodes '*CONT' Oxide
# Named polygons will be converted into electrodes
```

Realistic Processing

- Structure file…



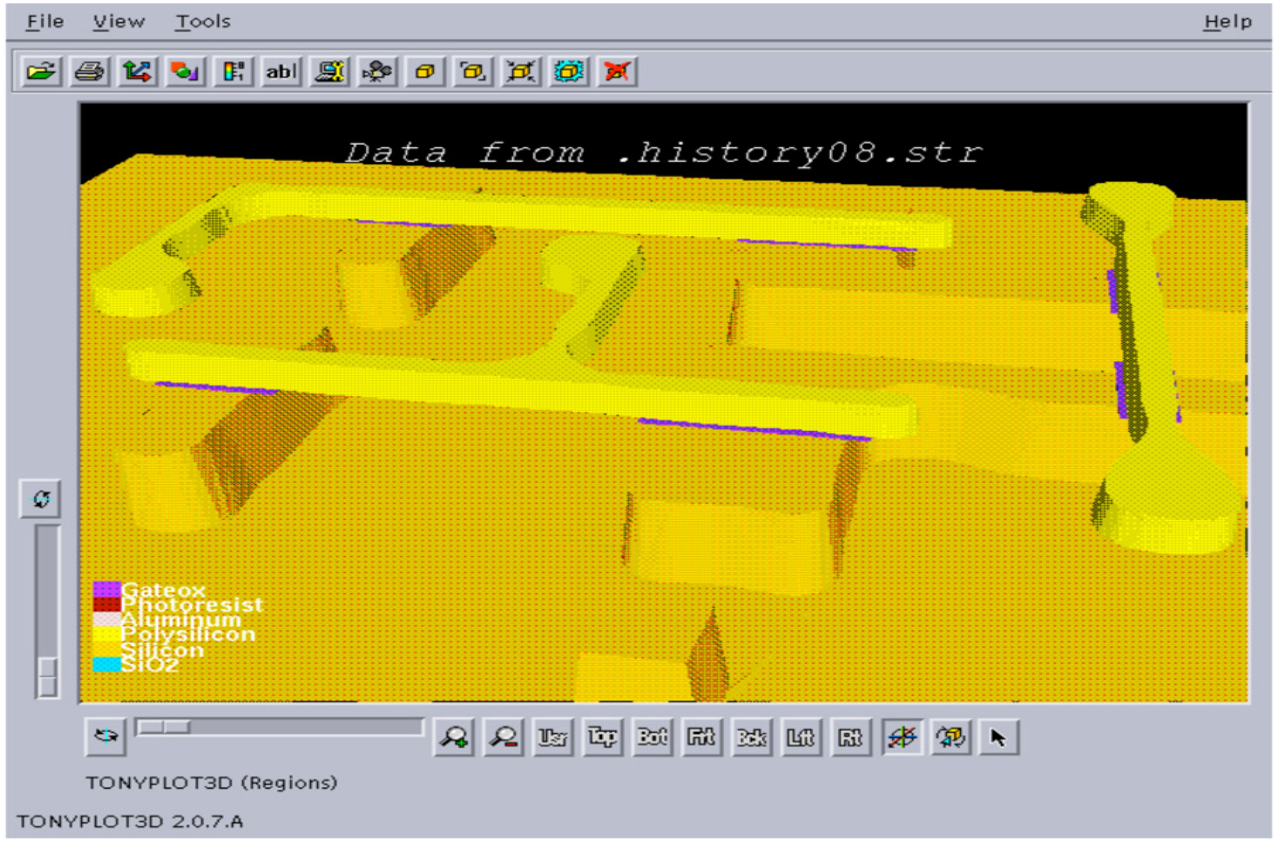
SEM Photograph of Typical Interconnect Geometry



Six memory cells of partially completed SRAM array after removal of oxide insulation.
SEM photograph (IBM)

Realistic Processing

- Structure file...



Parasitic Netlist

- Capacitance Netlist Comparison...

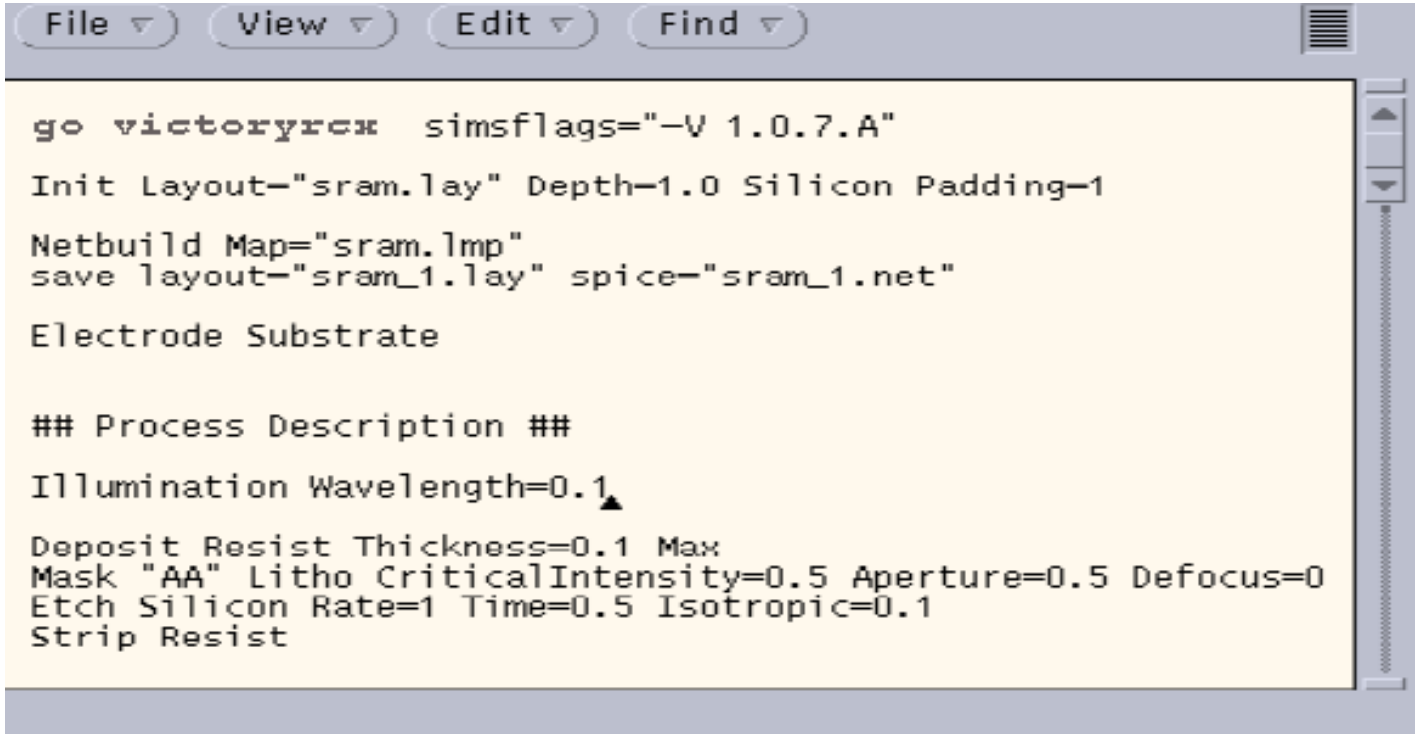
File View Edit Find

Compare Capacitance Netlist With and Without Realistic Processing

Description	Manhatton	Realistic	% Change
C1 cont0 cont1	1.73977e-18	1.25334e-18	28.0
C2 cont0 gate0	1.75647e-18	9.82503e-19	44.1
C3 cont0 cont3	1.75647e-18	9.82503e-19	44.1
C4 cont0 gate1	1.73977e-18	1.25334e-18	28.0
C5 cont0 cont5	2.49126e-17	1.6259e-17	34.7
C6 cont0 gate2	3.52452e-18	2.12673e-18	39.7
C7 cont0 bitbar	2.49126e-17	1.6259e-17	34.7
C8 cont0 wlm	3.52452e-18	2.12673e-18	39.7
C9 cont0 cont6	2.51231e-17	1.62988e-17	35.1
C10 cont0 gate3	3.52452e-18	2.12673e-18	39.7
		AVERAGE	36.8 %

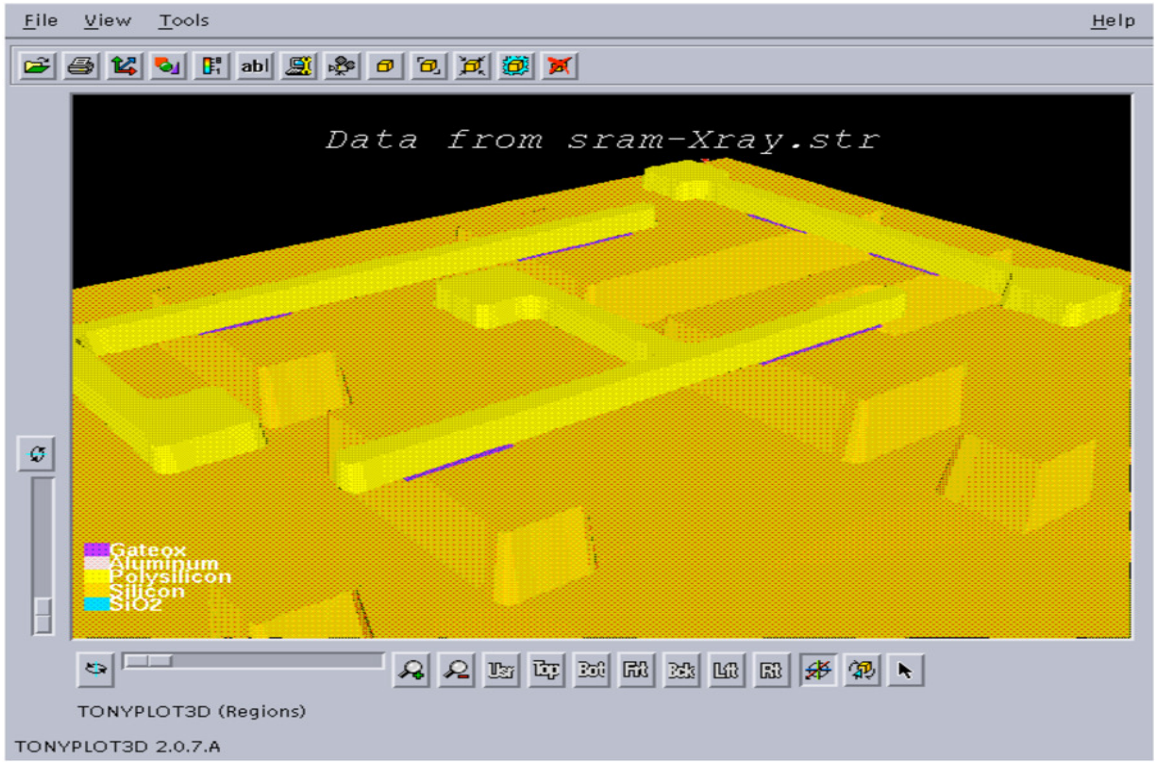
Realistic Processing

- The Effect of Changing ONLY the Wavelength of the Mask Aligner Lamp…
- The New Input File:



Realistic Processing

- The Effect of Changing ONLY the Wavelength of the Mask Aligner Lamp…
- The New Structure File:



Realistic Processing

- The Effect of Changing ONLY the Wavelength of the Mask Aligner Lamp…
- The New Net List and Comparison with Previous Netlists

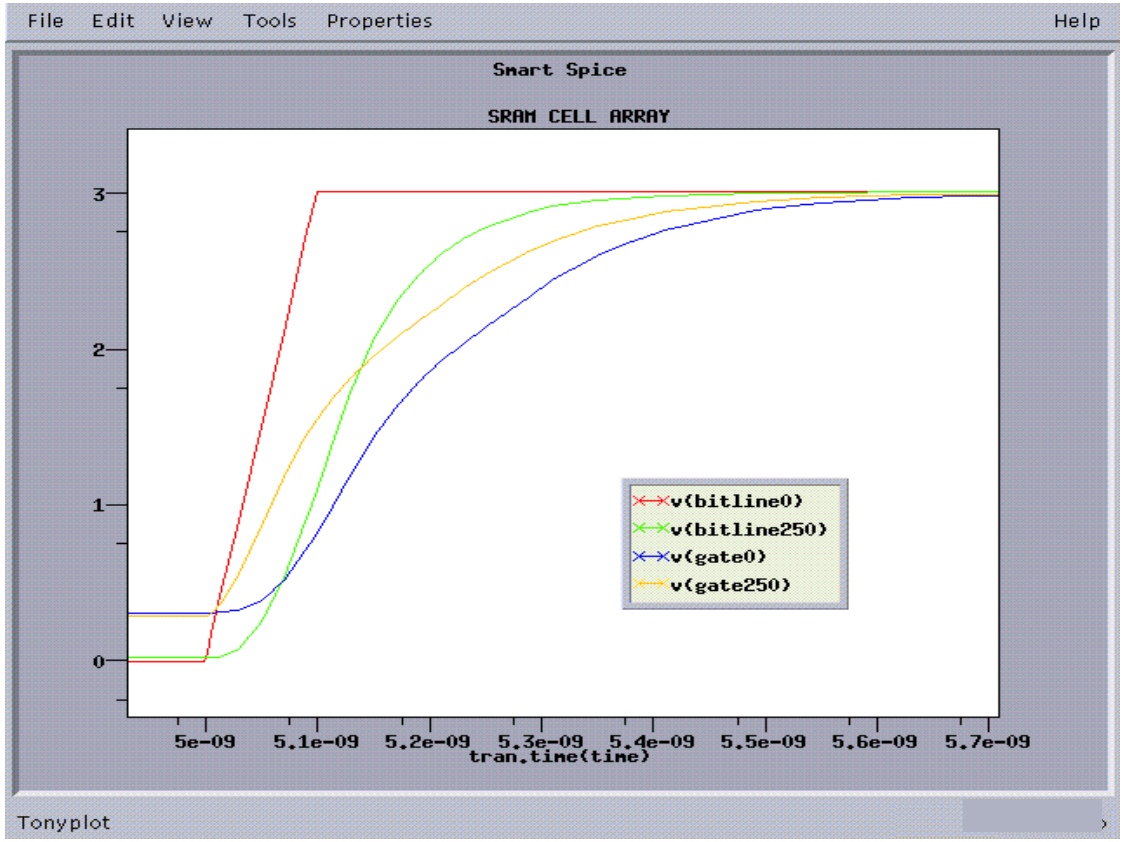
File ▽ View ▽ Edit ▽ Find ▽

Compare Capacitance Netlists...

Description	Manhatton	DeepUV (248nm)	%Change	Lambda=0.1um	%Change
C1 cont0 cont1	1.73977e-18	1.25334e-18	28.0	1.42615e-18	18.0
C2 cont0 gate0	1.75647e-18	9.82503e-19	44.1	1.16509e-18	33.7
C3 cont0 cont3	1.75647e-18	9.82503e-19	44.1	1.16509e-18	33.7
C4 cont0 gate1	1.73977e-18	1.25334e-18	28.0	1.42615e-18	18.0
C5 cont0 cont5	2.49126e-17	1.6259e-17	34.7	1.7085e-17	31.4
C6 cont0 gate2	3.52452e-18	2.12673e-18	39.7	2.30239e-18	34.7
C7 cont0 bitbar	2.49126e-17	1.6259e-17	34.7	1.7085e-17	31.4
C8 cont0 wlm	3.52452e-18	2.12673e-18	39.7	2.30239e-18	34.7
C9 cont0 cont6	2.51231e-17	1.62988e-17	35.1	1.71823e-17	31.6
C10 cont0 gate3	3.52452e-18	2.12673e-18	39.7	2.30239e-18	34.7
		AVERAGE	36.8 %		30.2 %

SPICE Simulation

- 250 SRAM cells were chained together to analyze timing implications



Conclusion

- Victory RCx Pro should be used for parasitic extraction where MAXIMUM ACCURACY is required (no simplifications)
- Use Victory RCx Pro to Optimize before processing
- Input Requirements:
  - Mask Layouts
  - Process Flows

Conclusion (con’t)

- Victory RXc Pro Includes:
  - Photo-Lithography Effects
  - Physical Deposition Models
  - Physical Etching Models
- Output:
  - Full parasitic capacitance SPICE netlist
  - Full parasitic resistance SPICE netlist