SILVACO
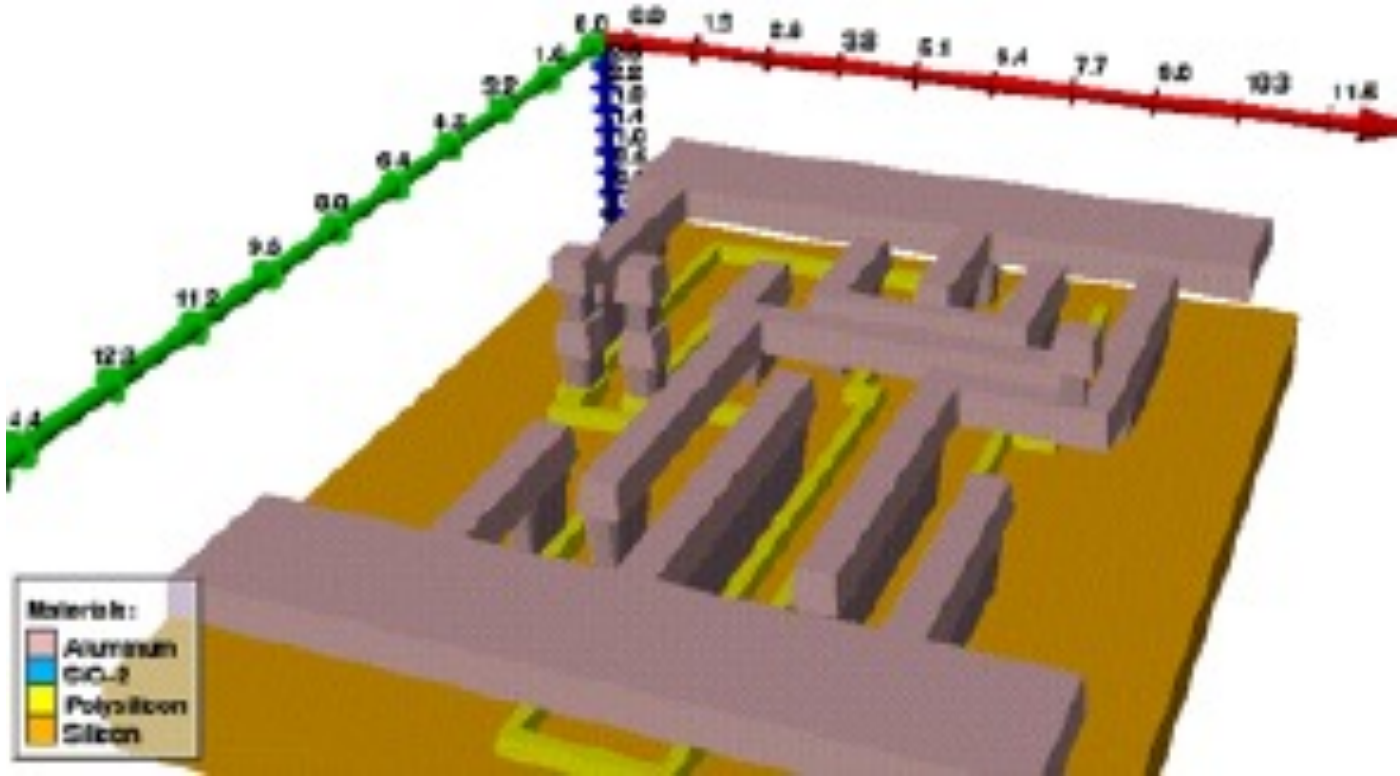
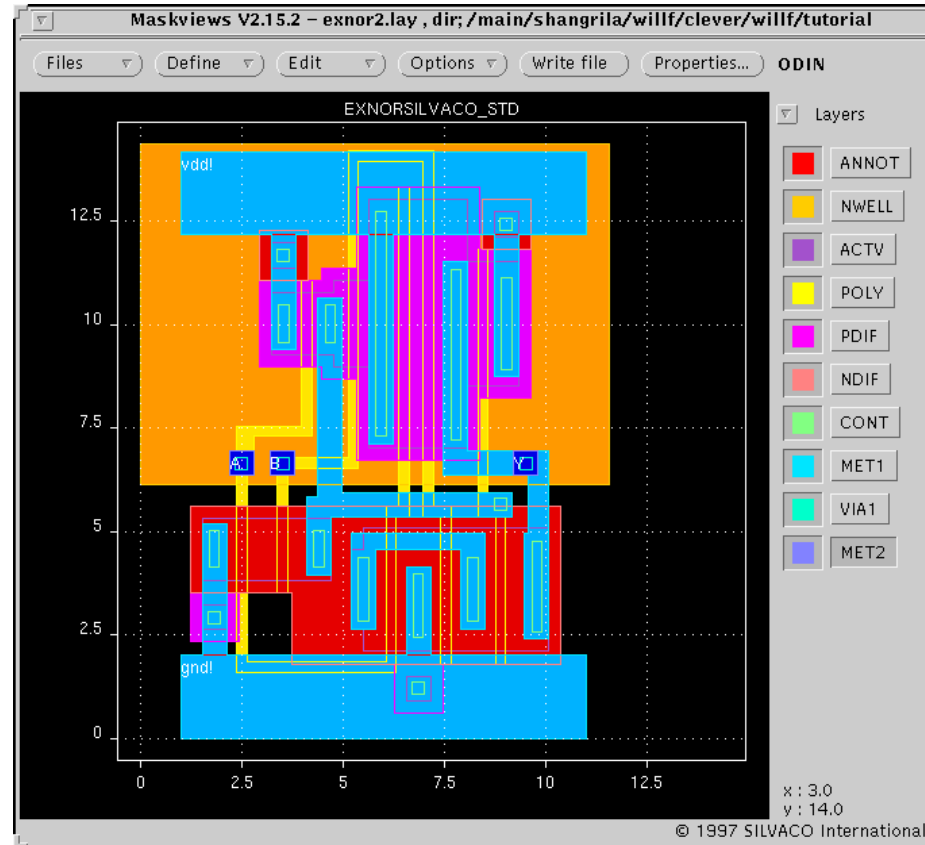# Victory RCx Pro: Physics-Based Parasitic Extraction

Application Examples

Exclusive NOR Cell Application
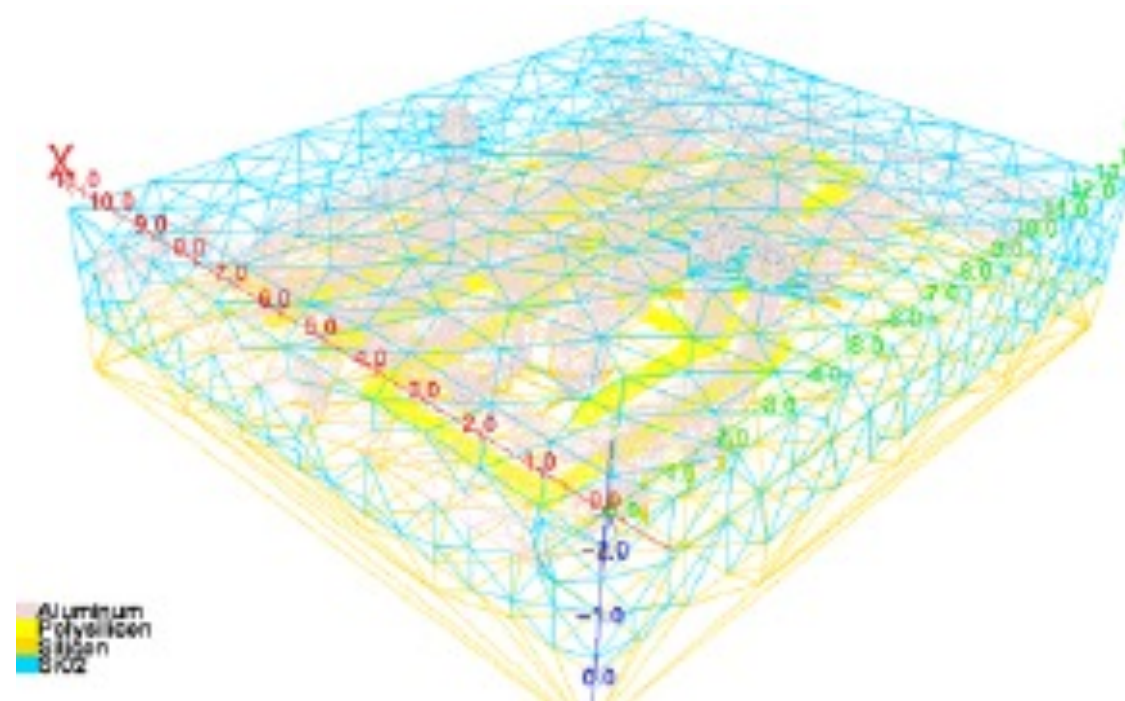

Accurate parasitic extraction for an exclusive NOR cell requires realistic interconnect geometries.

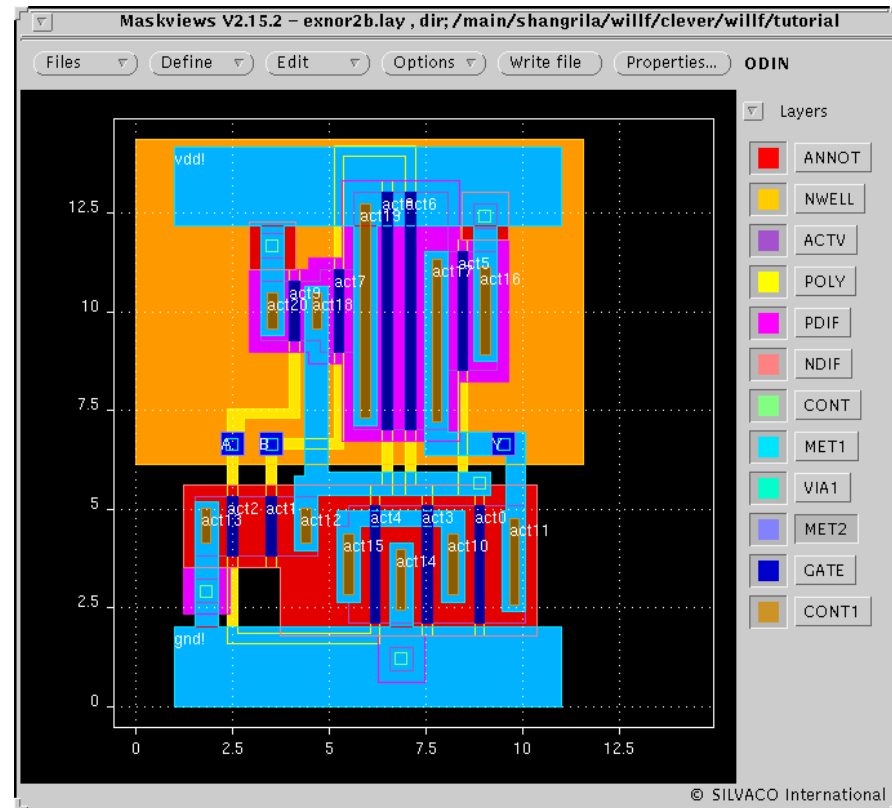# Exclusive NOR Cell Application (con't)

Original GDS-II layout of exclusive NOR cell.
Node labels are read from GDS-II file.

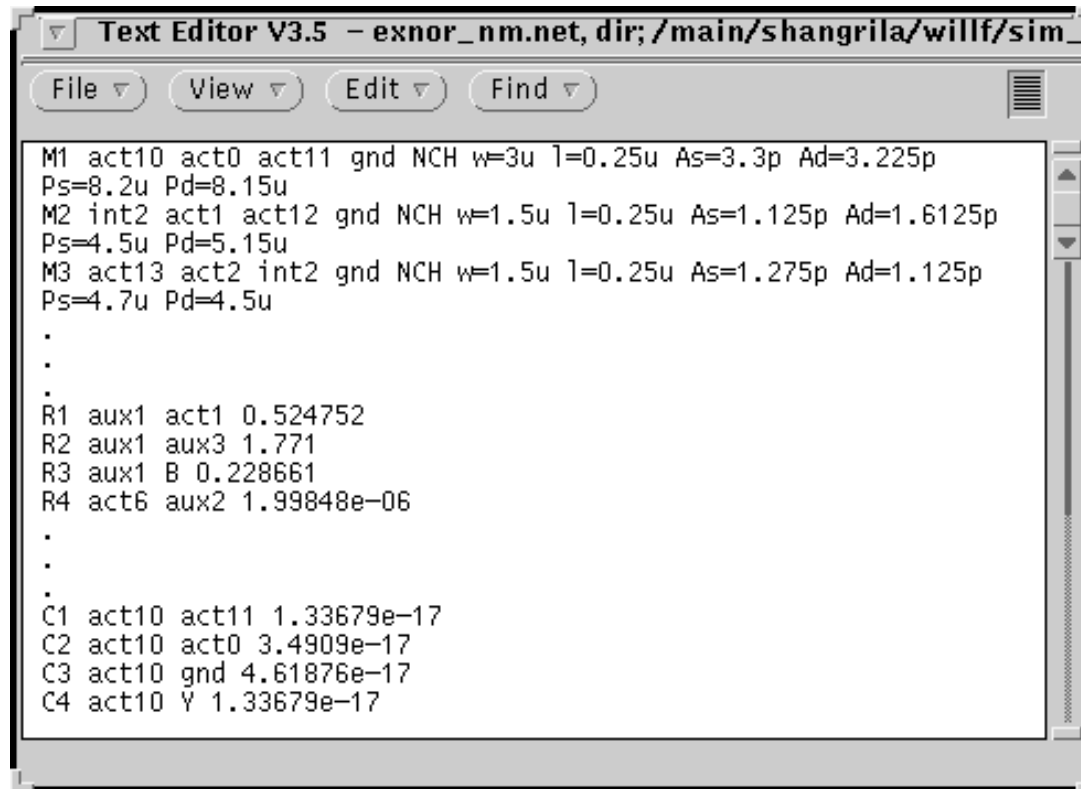# Exclusive NOR Cell Application (con't)

Accurate parasitic extraction for an exclusive NOR cell requires realistic interconnect geometries.

Exclusive NOR Cell Application (con't)

EXNOR layout annotated with internal node locations. The internal nodes are used for back-annotation to the netlist.
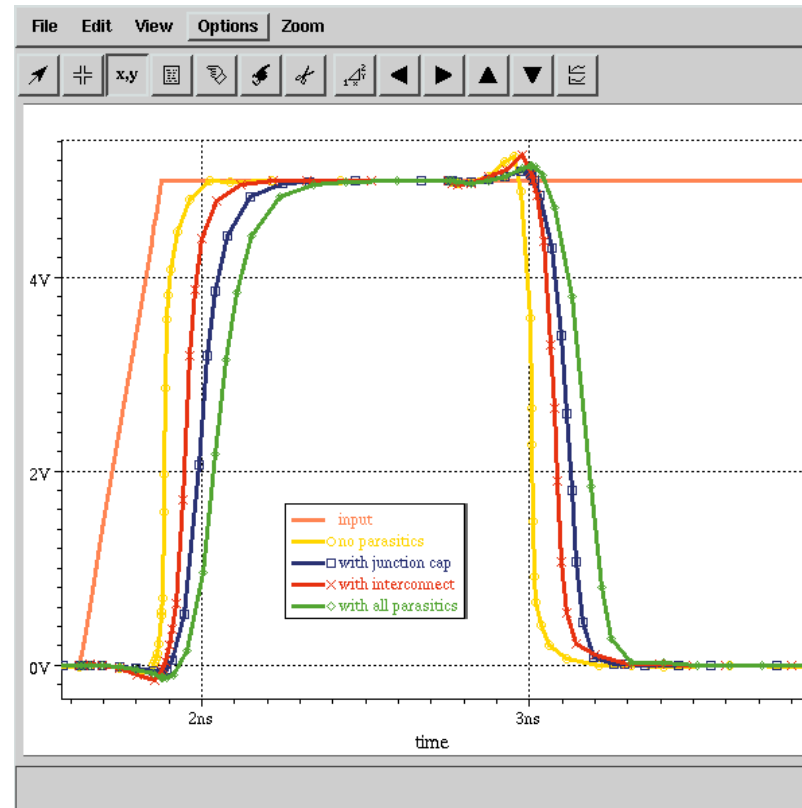
Exclusive NOR Cell Application (con't)


```
Text Editor V3.5 – exnor_nm.net, dir;/main/shangrila/willf/sim_

File ▽    View ▽    Edit ▽    Find ▽                        ▤

M1 act10 act0 act11 gnd NCH w=3u l=0.25u As=3.3p Ad=3.225p
Ps=8.2u Pd=8.15u
M2 int2 act1 act12 gnd NCH w=1.5u l=0.25u As=1.125p Ad=1.6125p
Ps=4.5u Pd=5.15u
M3 act13 act2 int2 gnd NCH w=1.5u l=0.25u As=1.275p Ad=1.125p
Ps=4.7u Pd=4.5u
.
.
.
R1 aux1 act1 0.524752
R2 aux1 aux3 1.771
R3 aux1 B 0.228661
R4 act6 aux2 1.99848e-06
.
.
.
C1 act10 act11 1.33679e-17
C2 act10 act0 3.4909e-17
C3 act10 gnd 4.61876e-17
C4 act10 Y 1.33679e-17
```
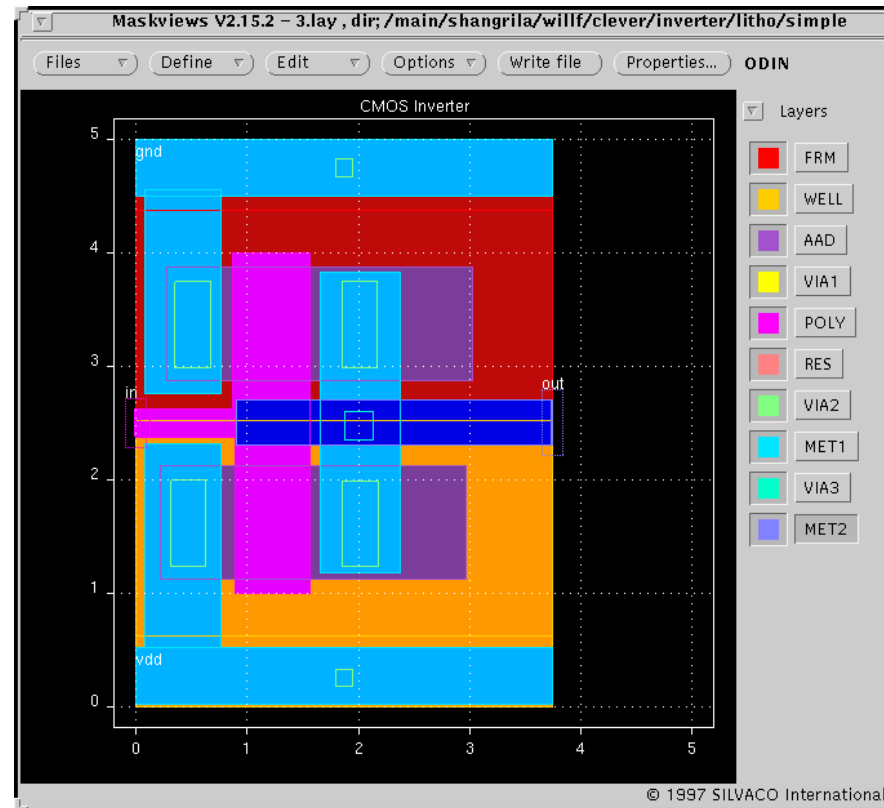
EXNOR layout annotated with internal node locations.
The internal nodes are used for back-annotation to the netlist.

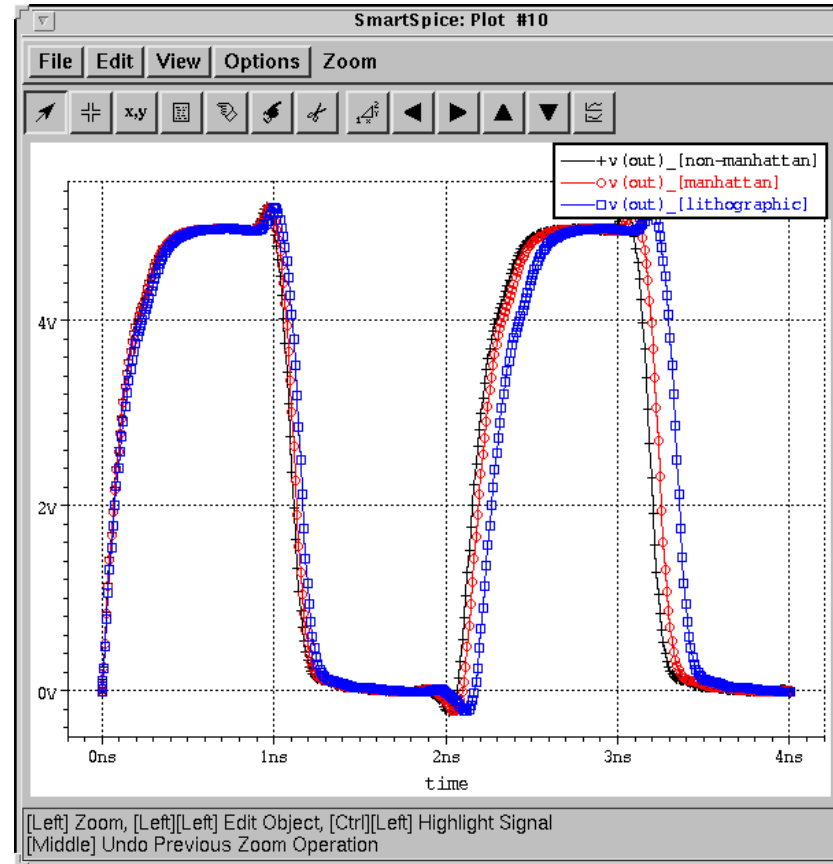**SILVACO**

Exclusive NOR Cell Application (con't)

SPICE simulation showing the effect of interconnect parasitics on timing of the EXNOR cell.
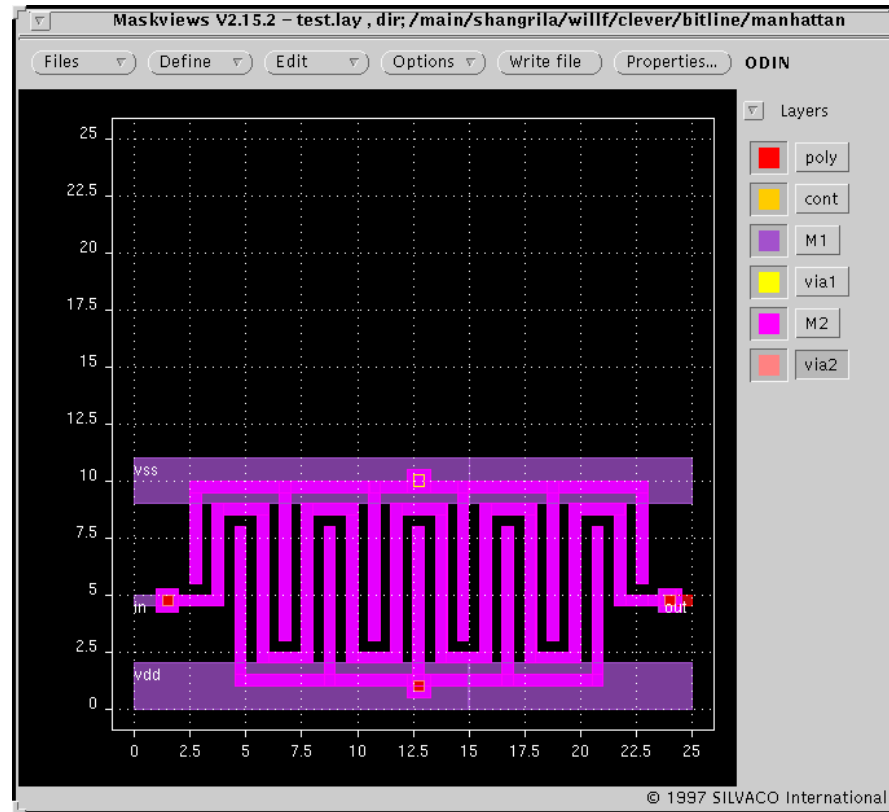
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CMOS Inverter Application

CMOS inverter layout used to compare different interconnect geometry models.
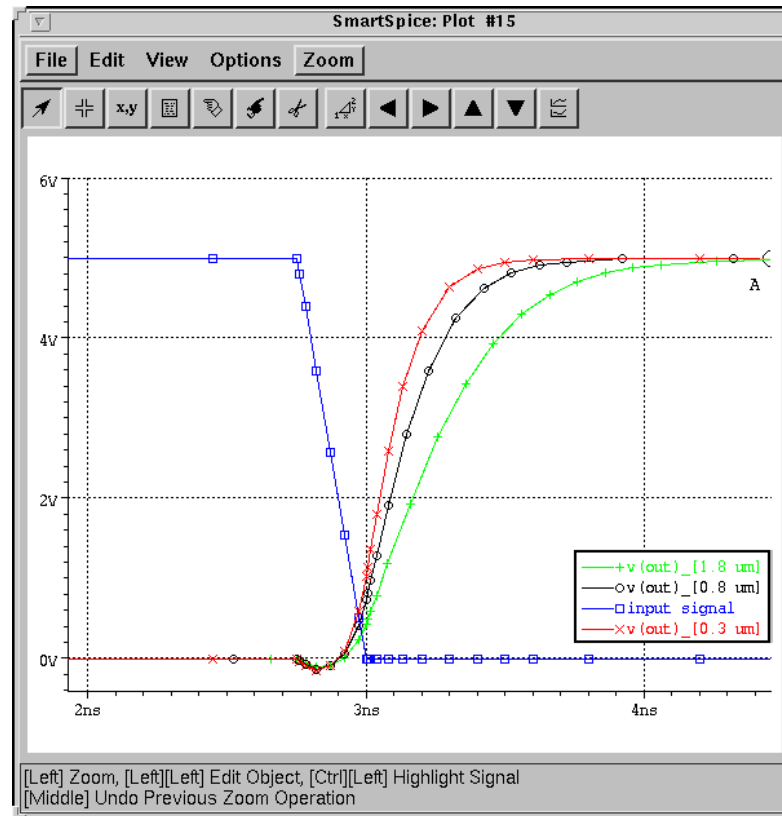
CMOS Inverter Application (con't)

Effect of using idealized geometries vs. realistic interconnect
process simulation on ring oscillator gate delay.

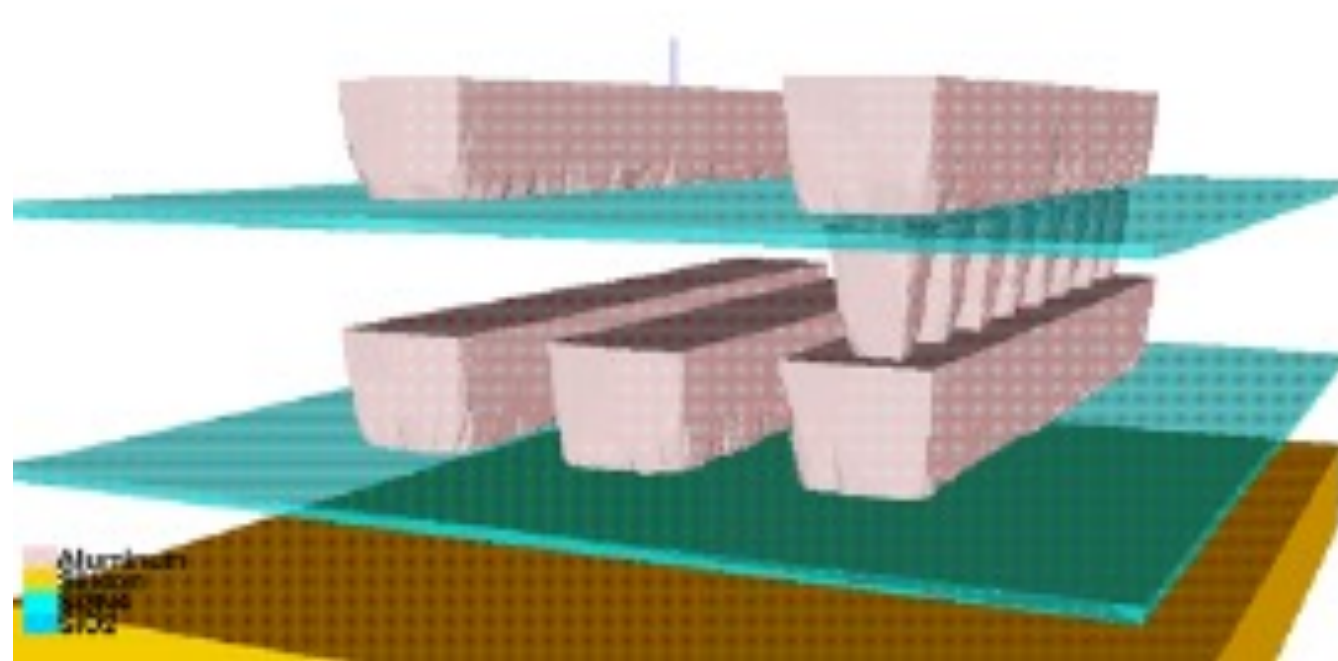# CMOS Inverter Application (con't)

Metal serpentine used to examine metal width effects.

CMOS Inverter Application (con't)

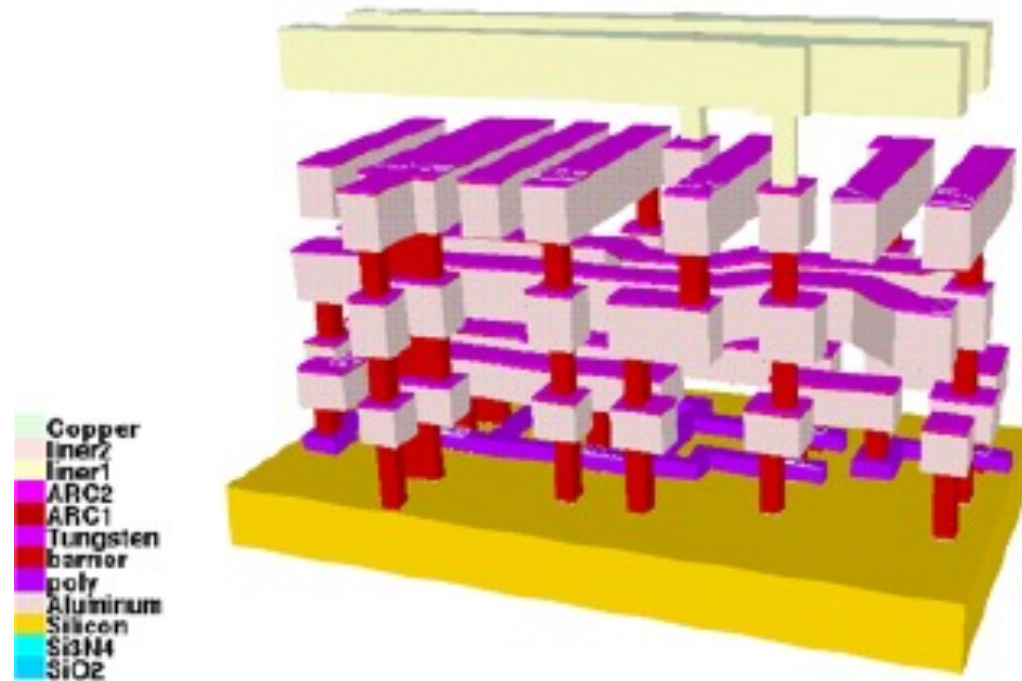Effects of different metal widths on inverter's gate delay are plotted.

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CMOS Inverter Application (con't)

Simulation of Aluminum Dual Damascene process with nitride etch stops.
Victory RCx Pro can handle arbitrary process complexity.

SRAM Application

Copper
liner2
liner1
ARC2
ARC1
Tungsten
barrier
poly
Aluminum
Silicon
Si3N4
SiO2

SRAM cell with 4 metal layers plus polysilicon. Each metal layer is composed of multiple material layers which are correctly modeled by Victory RCx Pro for accurate resistance extraction.

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SRAM Application (con't)
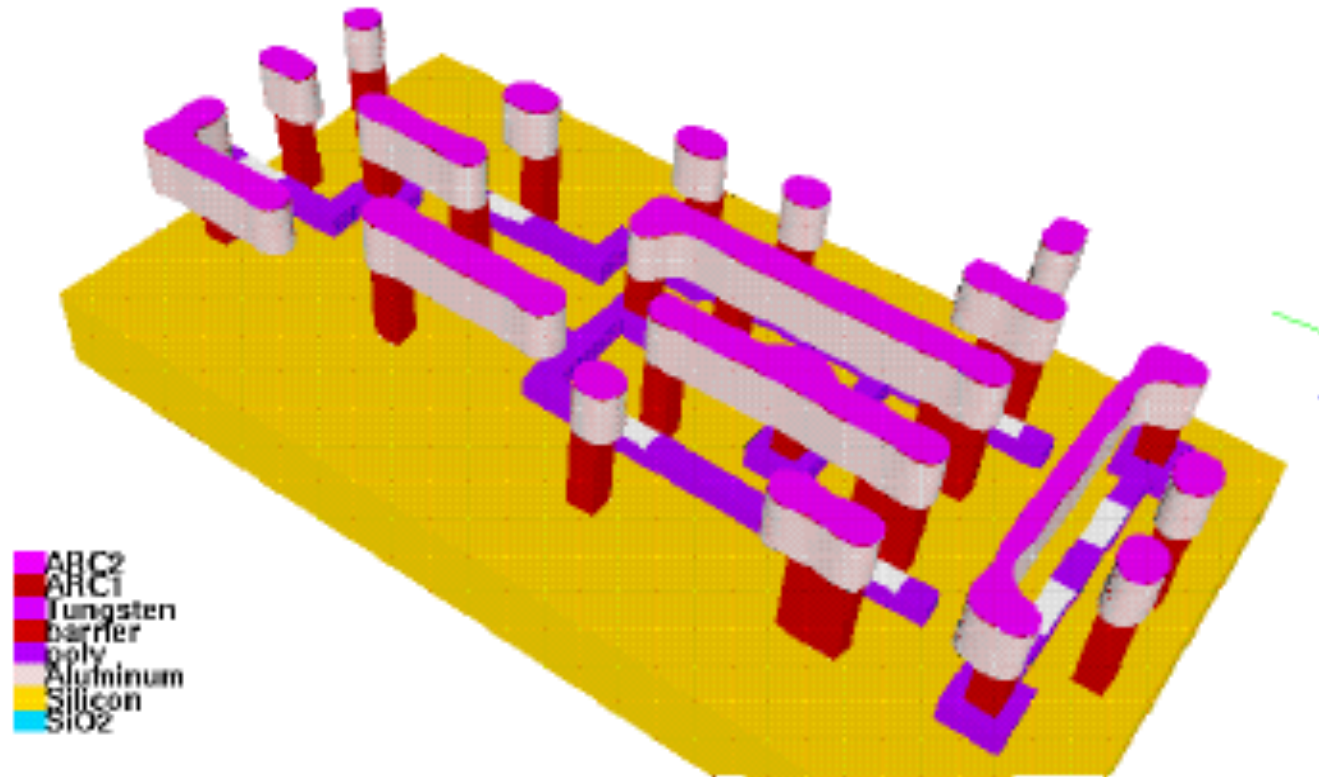
Lithography effect on Metal 1 geometry of an SRAM cell. Significant differences in metal geometry versus an idealized case are seen affecting both capacitance and resistance.

Conclusion

- Victory RCx Pro can be used to examine and optimize interconnect processing and layout effects on circuit timing for any arbitrary small cells

- Full photolithographic and 3D processing capability coupled with the use of field solvers results in the highest possible accuracy for cell level R.C. extraction

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