SILVACO

Victory RCx Pro
RC – Extractor for 3D Structures

Technology-Driven Parasitic Extraction Tool

Applications

- Victory RCx fits well as an RC extraction tool in the following markets:
- Deep submicron CMOS
  - Realistic 3D back end process simulations and accurate interconnect simulation with user selected tolerance
  - Accurate via detailed capacitance and process analysis of individual problematic features, such as 45 nm via structures
- Flat Panel LCD and TFT circuits
  - Special features to deal with high aspect ratio structure
  - SED Television technology
- Memory manufacturing
  - SRAM and Flash Memory cell
- MEMS simulation
  - Systems-on-a-chip brings together silicon-based microelectronics with micromachining technology

Benefits

- Advanced lithography and realistic etch deposition models are used to create realistic structure
- Conductor and Insulator Field Solvers based for high accuracy capacitances and resistances calculation
- Accurately solves critical 3D back end process steps (e.g. dual damascene, thin layer deposition)
- Increase productivity with fast, multi-threaded 3D process simulation
- Optimize circuit performance as a function of back end process parameters and layout parameters
- Solve process integration issues due to layout design errors
- High level of automation (integrated in the VWF)

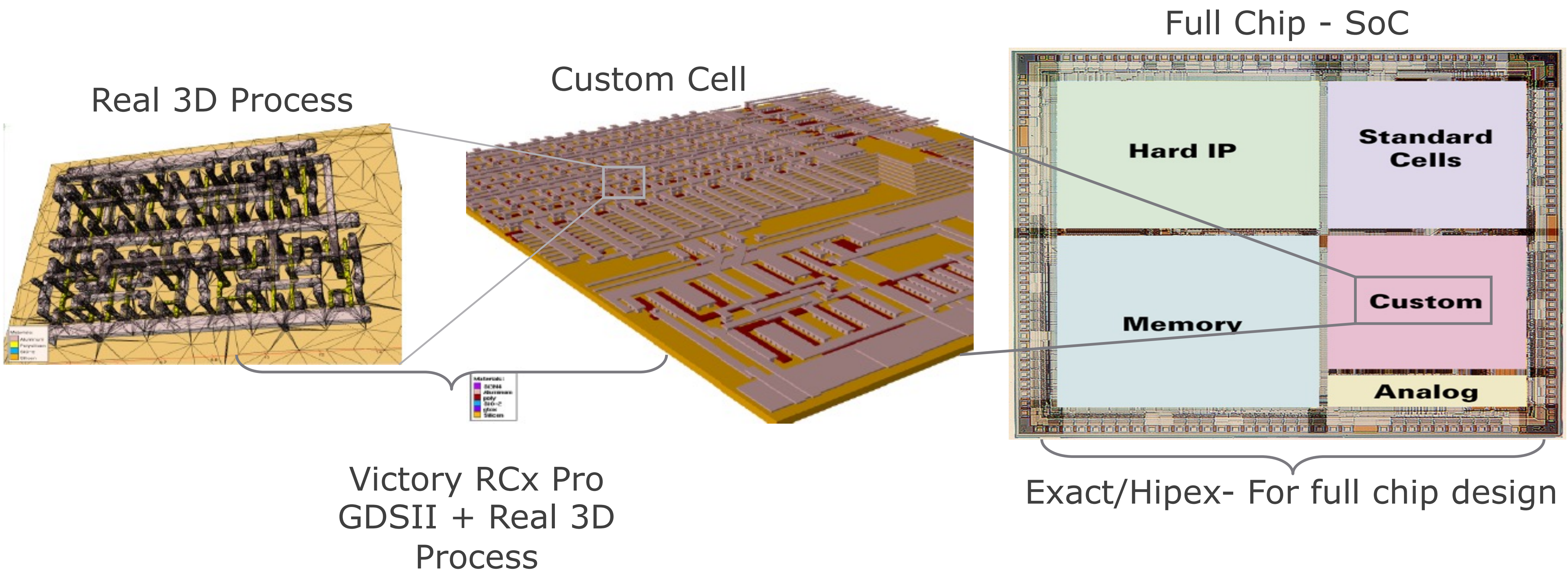
Advantages

- No restriction on geometry size – 65nm, 45nm and below
- Realistic Structure Generation – suitable for all technologies and arbitrary 3D shapes
- Only RC extractor in the industry capable of reproducing the lithographic effects of Optical Proximity Correction (OPC) sub wavelength effects, phase-shifts mask (PSM), misalignment, defocus, and ΔCD
- True 3D, mask driven process simulation
- Realistic deposition, etch and photolithography
- Netlist extractor to extract active device SPICE netlist
- User selectable boundary condition
- User definable materials names and properties

Advantages (con’t)

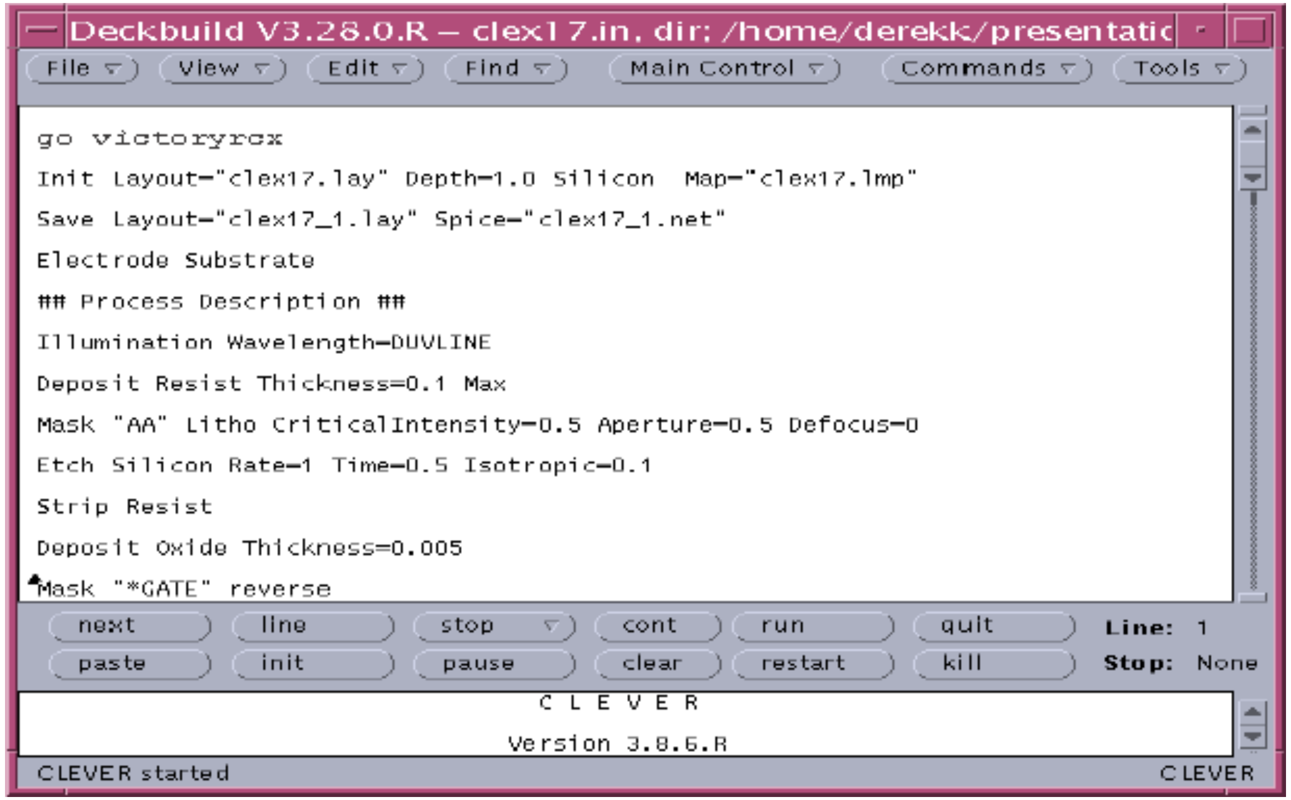
- Automatic back annotation of field solved resistances and capacitances onto extracted active device netlist for immediate SPICE analysis
- Full 3D field solver engine directly calculates parasitic RC extraction for best accuracy and handle dummies
- Automatic grid generation and refinement during 3D field solver calculation of capacitance and resistance
- Versatile – small cells using fully realistic 3D processing or larger cells using geometric processing
- User-defined tolerance control on extraction accuracy
- 2D/3D structure Viewer (TonyPlot2D/3D)
- Post-processing tools to make capacitance and resistance models and optimization
- Symmetric boundary condition to allow users to perform Cyclic Simulations
- Selective area parasitic extraction enables maximum accuracy for critical layout windows

Victory RCx Pro – Simulator



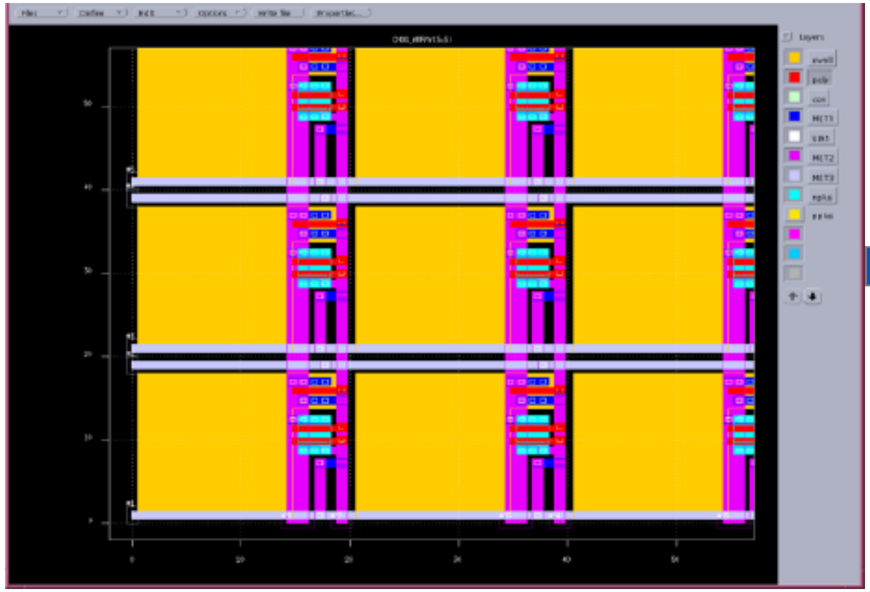
Victory RCx Pro – Simulator

- Simple intuitive Mask Driven process simulation syntax
- Easy to learn and use
- User friendly input file development and runtime environment

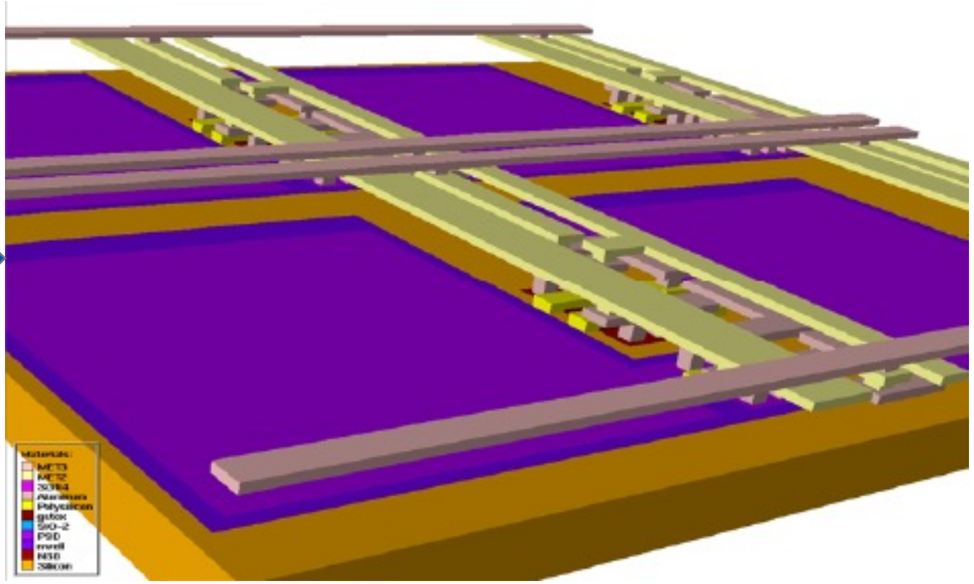


Victory RCx Pro – Layout Driven

- 3D structures created from Mask Driven intuitive process commands



GDS2 Mask Layout



3D Structure

Victory RCx Pro – Tracking Fronts in Etch/Deposition

- Victory RCx Pro simulates realistic geometric etch and deposition steps very efficiently with unstructured tetrahedral mesh - the developed algorithm combines the efficiency of string methods and the robustness of Level Set methods

A generic model for etch and deposit

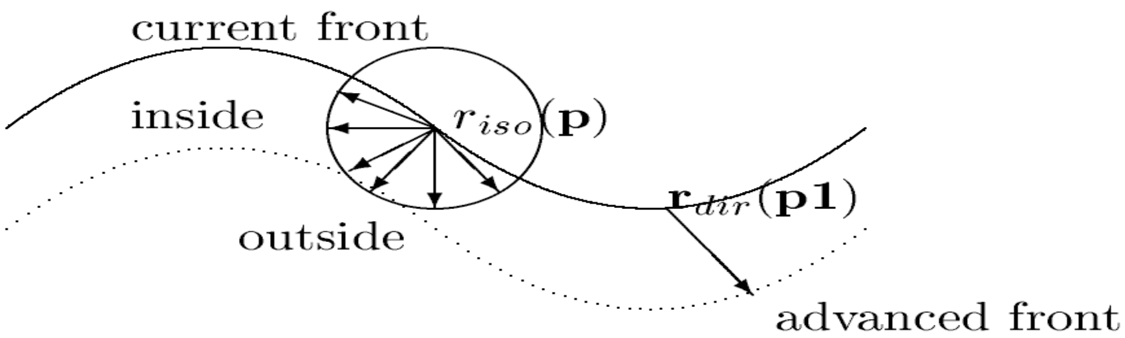
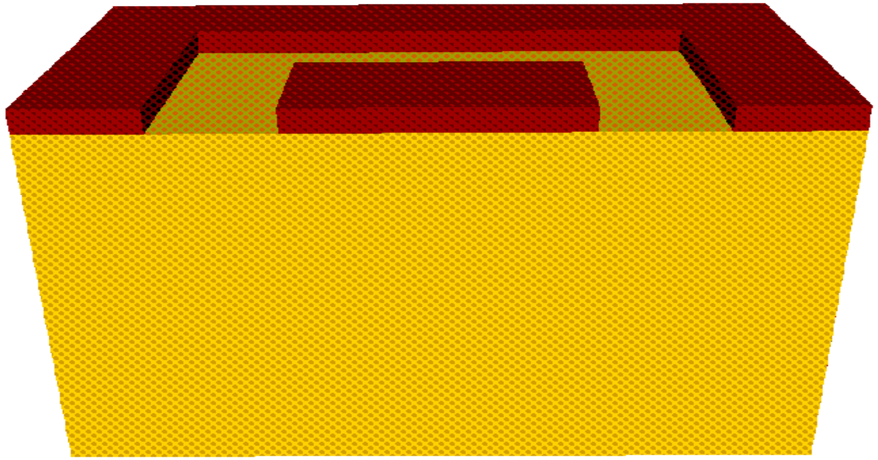


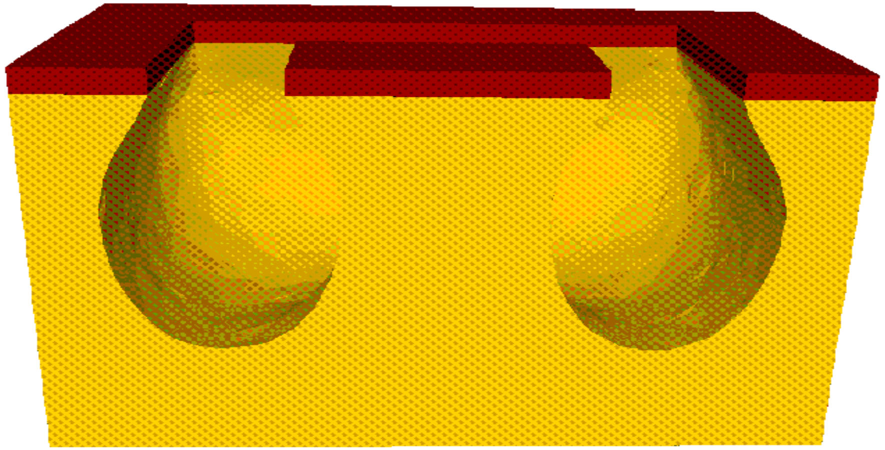
Illustration for one step of the moving front; $r_{iso}(p)$ is isotropic etch rate at point p, and $r_{dir}(p1)$ is directional etch rate at point p1.

Victory RCx Pro – Tracking Fronts in Etch/Deposition

- Example – creation and refill of a trench structure



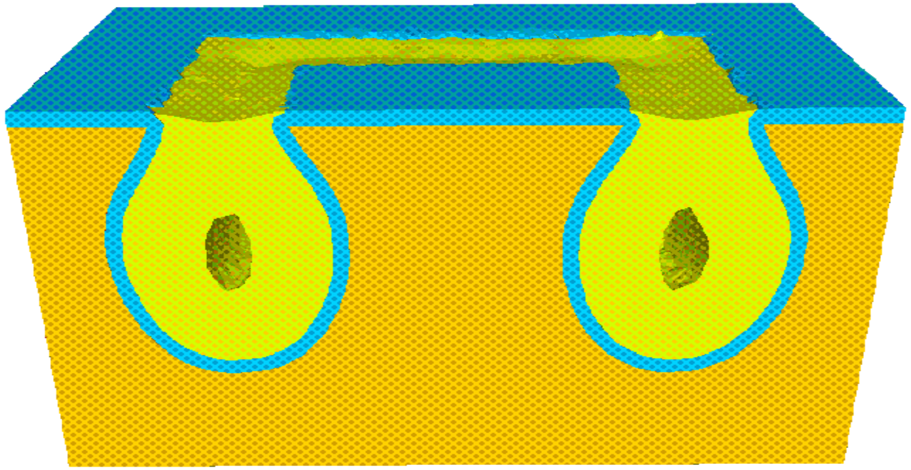
Patterning of photoresist.



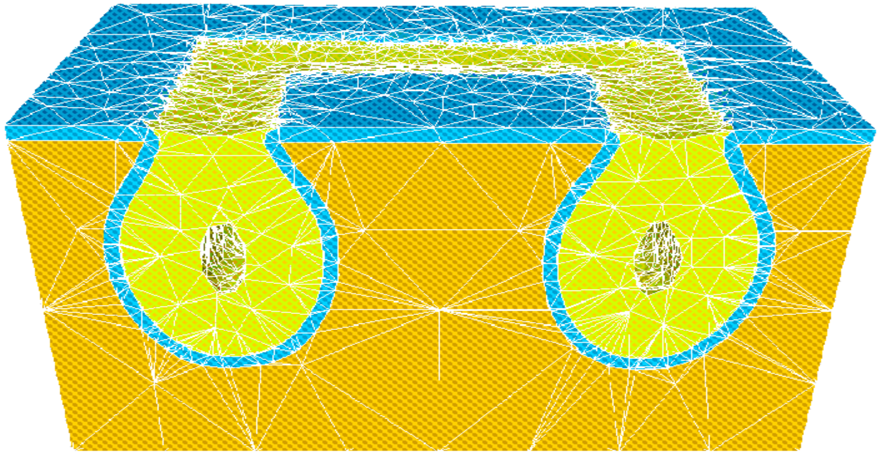
Directional etching; r_{dir} is determined by the visible "cone" from above.

Victory RCx Pro – Tracking Fronts in Etch/Deposition

- Example – creation and refill of a trench structure



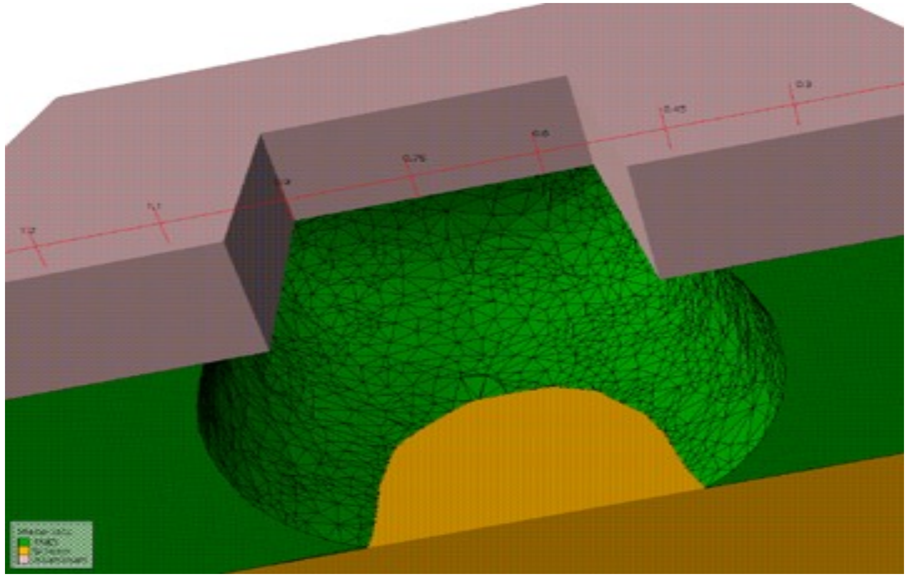
Trench refill; illustration of void creation.

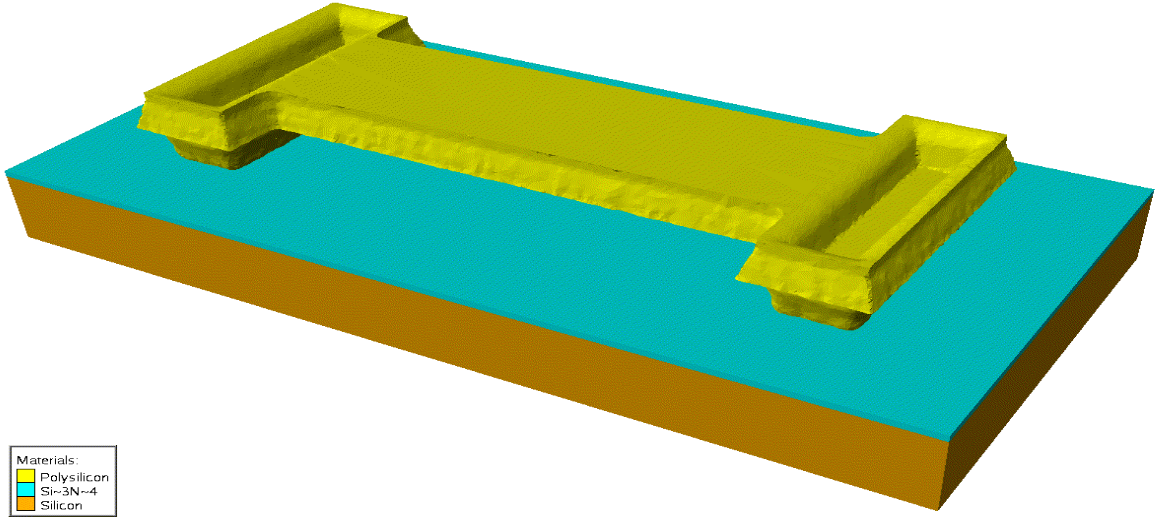


Final trench structure with mesh.

Victory RCx Pro – Tracking Fronts in Etch/Deposition

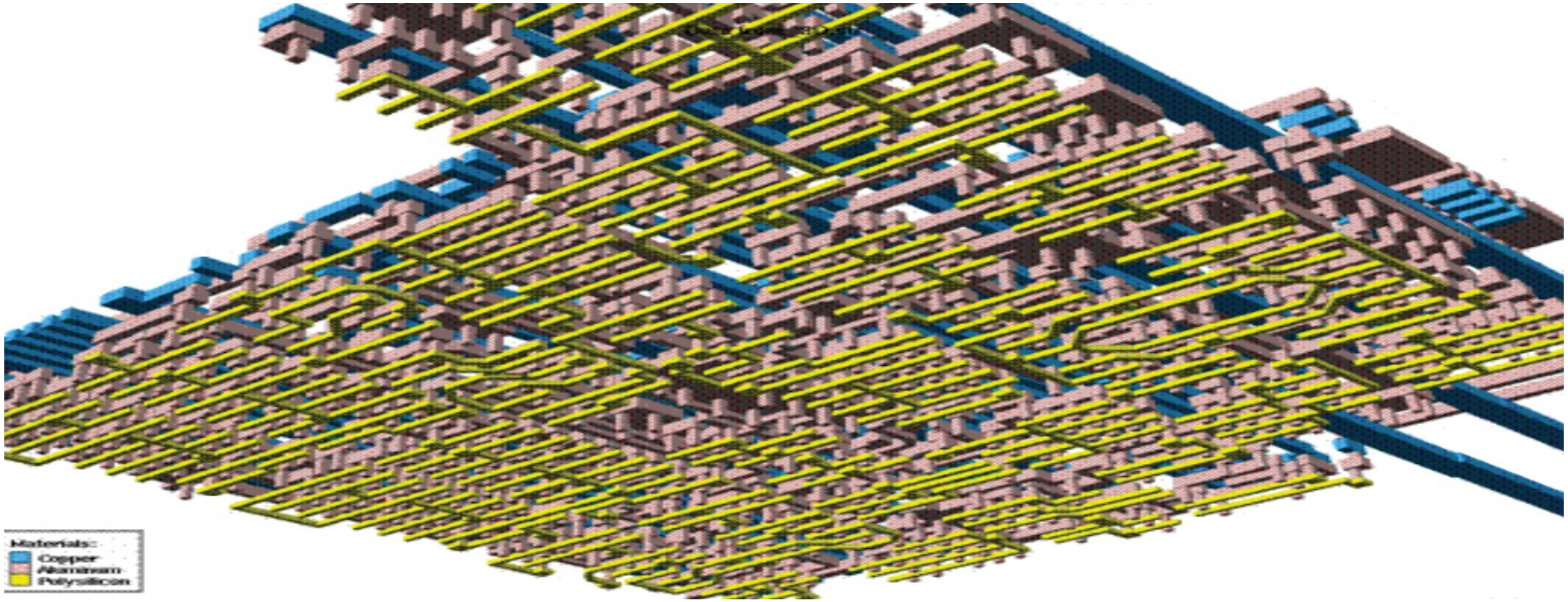
- Complex etching capability
- Difficult Etch/Deposit Combinations Possible





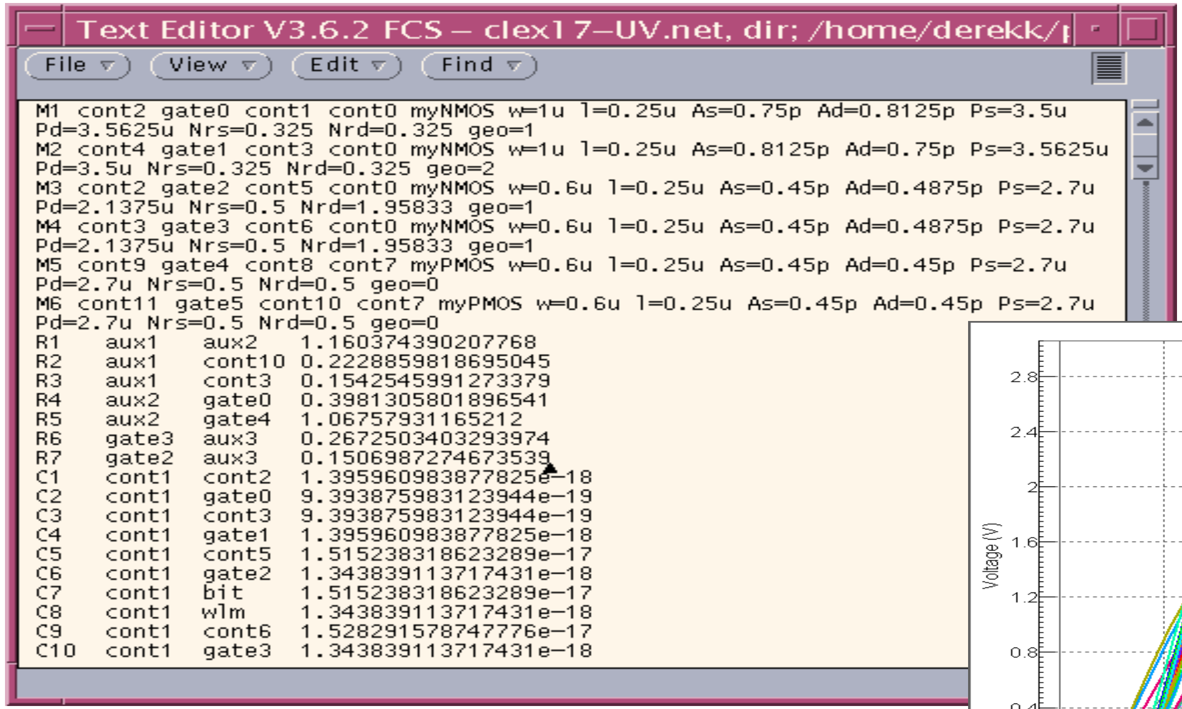
Victory RCx Pro – Tracking Fronts in Etch/Deposition

- Optional geometric deposition/etch allows much larger circuits to be simulated using the same memory



Victory RCx Pro – Back Annotation

- Automated annotated SPICE netlist generation

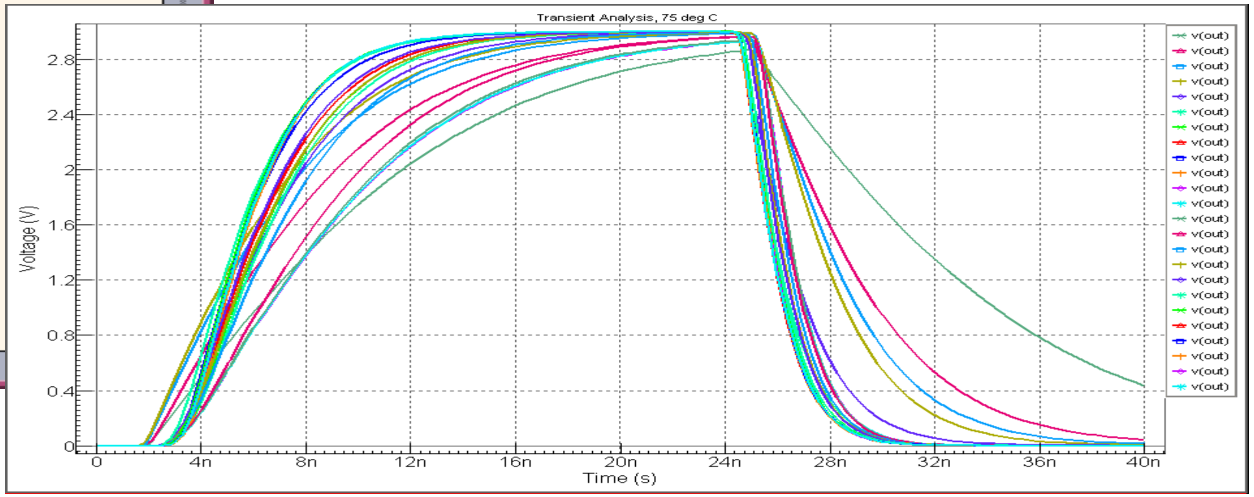


Text Editor V3.6.2 FCS – clex17–UV.net, dir; /home/derekk/|

File View Edit Find

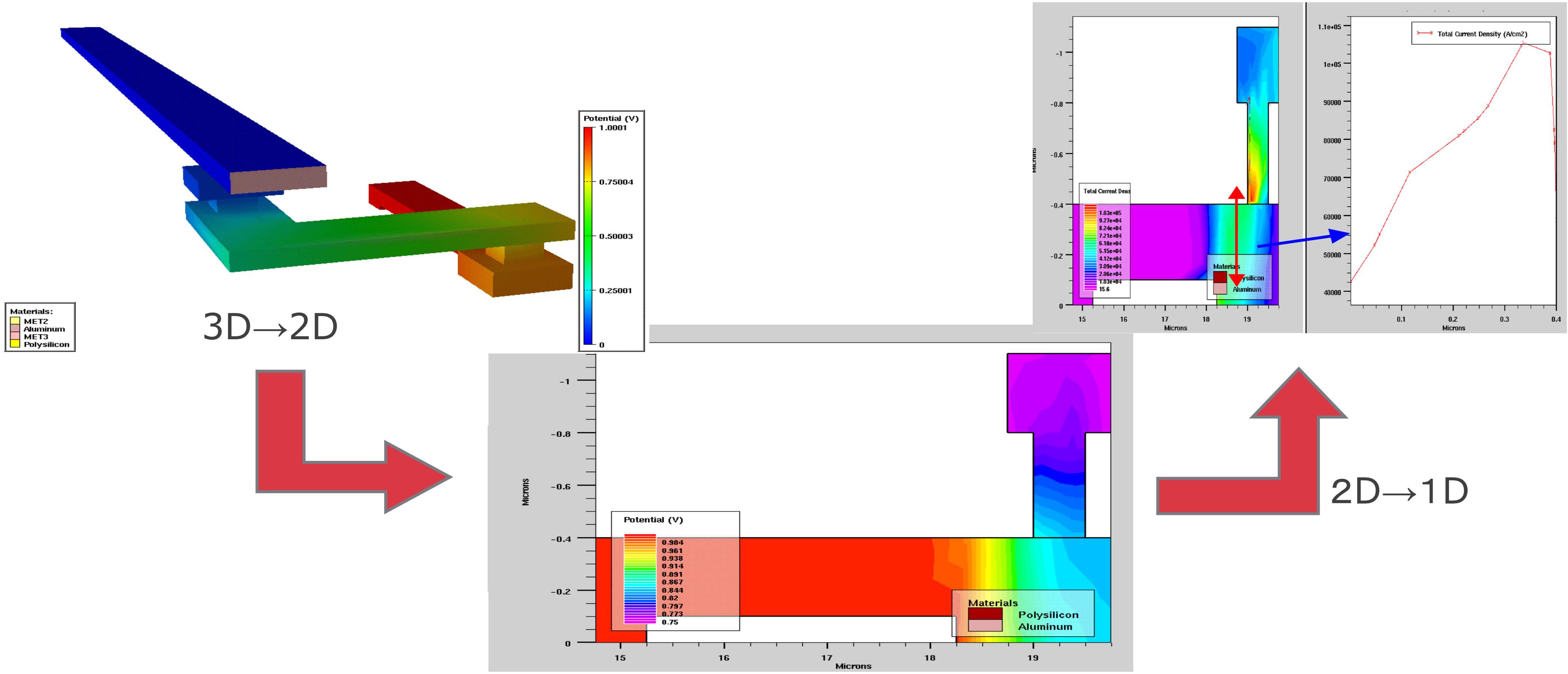
```
M1 cont2 gate0 cont1 cont0 myNMOS w=1u l=0.25u As=0.75p Ad=0.8125p Ps=3.5u
Pd=3.5625u Nrs=0.325 Nrd=0.325 geo=1
M2 cont4 gate1 cont3 cont0 myNMOS w=1u l=0.25u As=0.8125p Ad=0.75p Ps=3.5625u
Pd=3.5u Nrs=0.325 Nrd=0.325 geo=2
M3 cont2 gate2 cont5 cont0 myNMOS w=0.6u l=0.25u As=0.45p Ad=0.4875p Ps=2.7u
Pd=2.1375u Nrs=0.5 Nrd=1.95833 geo=1
M4 cont3 gate3 cont6 cont0 myNMOS w=0.6u l=0.25u As=0.45p Ad=0.4875p Ps=2.7u
Pd=2.1375u Nrs=0.5 Nrd=1.95833 geo=1
M5 cont9 gate4 cont8 cont7 myPMOS w=0.6u l=0.25u As=0.45p Ad=0.45p Ps=2.7u
Pd=2.7u Nrs=0.5 Nrd=0.5 geo=0
M6 cont11 gate5 cont10 cont7 myPMOS w=0.6u l=0.25u As=0.45p Ad=0.45p Ps=2.7u
Pd=2.7u Nrs=0.5 Nrd=0.5 geo=0
R1   aux1   aux2   1.160374390207768
R2   aux1   cont10 0.2228859818695045
R3   aux1   cont3  0.1542545991273379
R4   aux2   gate0  0.3981305801896541
R5   aux2   gate4  1.06757931165212
R6   gate3  aux3   0.2672503403293974
R7   gate2  aux3   0.1506987274673539
C1   cont1  cont2  1.395960983877825e-18
C2   cont1  gate0  9.393875983123944e-19
C3   cont1  cont3  9.393875983123944e-19
C4   cont1  gate1  1.395960983877825e-18
C5   cont1  cont5  1.515238318623289e-17
C6   cont1  gate2  1.343839113717431e-18
C7   cont1  bit    1.515238318623289e-17
C8   cont1  wlm    1.343839113717431e-18
C9   cont1  cont6  1.528291578747776e-17
C10  cont1  gate3  1.343839113717431e-18
```

Immediate feedback on circuit speed following DOE process or layout modifications



Victory RCx Pro – Current Density

- Current density analysis

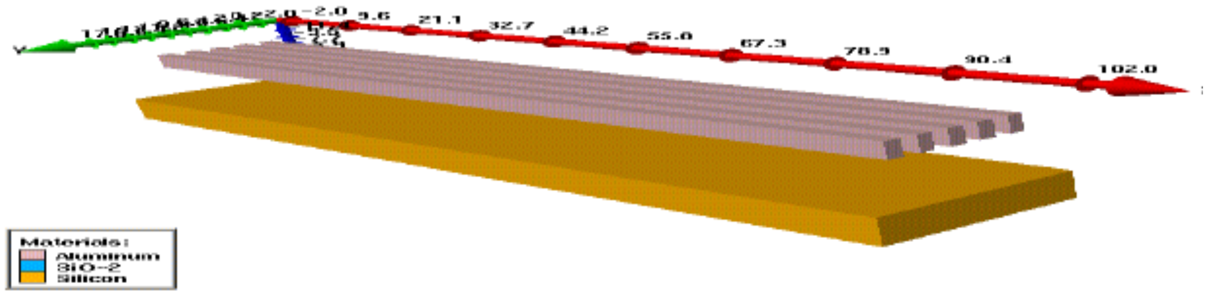


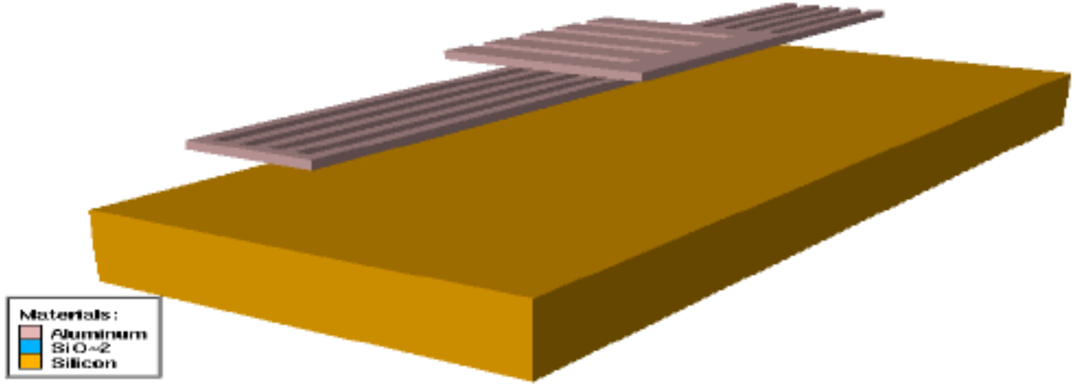
Case Studies

- Capacitance extraction on 83 layouts with, Victory RCx Pro, QuickCap and Stellar
- Deep submicron CMOS
- Flat panel
- Memory Cells
- MEMS simulation
- Local Interconnect

Capacitance Extraction on 83 Layouts

- Capacitance extraction with QuickCap, Victory RCx Pro and Stellar
- Layouts
  - Among the 83 layouts, we find 3 families :
  - Long parallel lines (73)
  - Combs (8)
  - Special process (2) (non-planar)





Capacitance Extraction on 83 Layouts

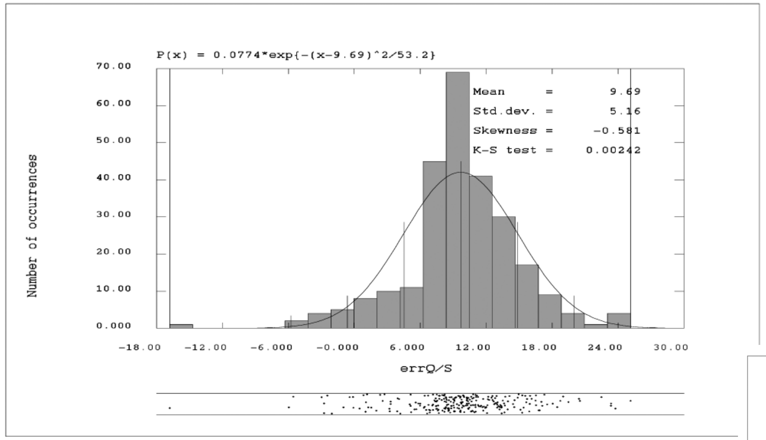
- The error is calculated as:

$$errX/Y = \frac{X - Y}{(X + Y)/2} \times 100$$

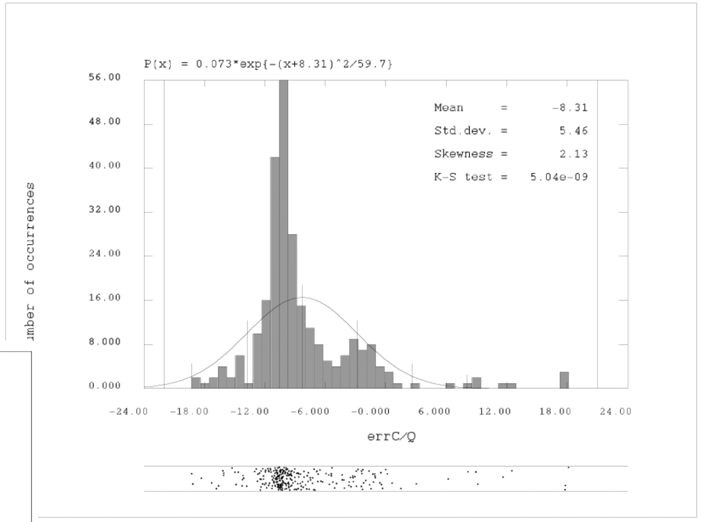
- The total number of capacitances extracted is 270
- Analysis
  - The analysis is made using Spayn
  - The data set of errors has been filtered (3 sigma filtering) and 261 values have been retained (96.67% of the total)
  - Errors are displayed in histogram fitted with a gaussian distribution

Capacitance Extraction on 83 Layouts

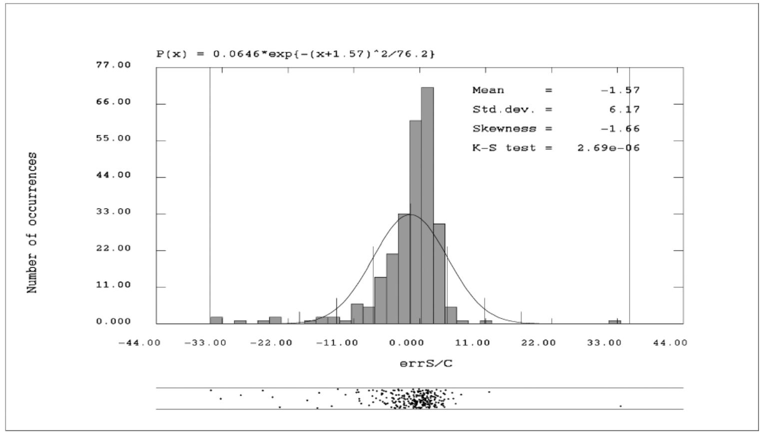
Quickcap vs Stellar



Quickcap vs Victory RCx Pro

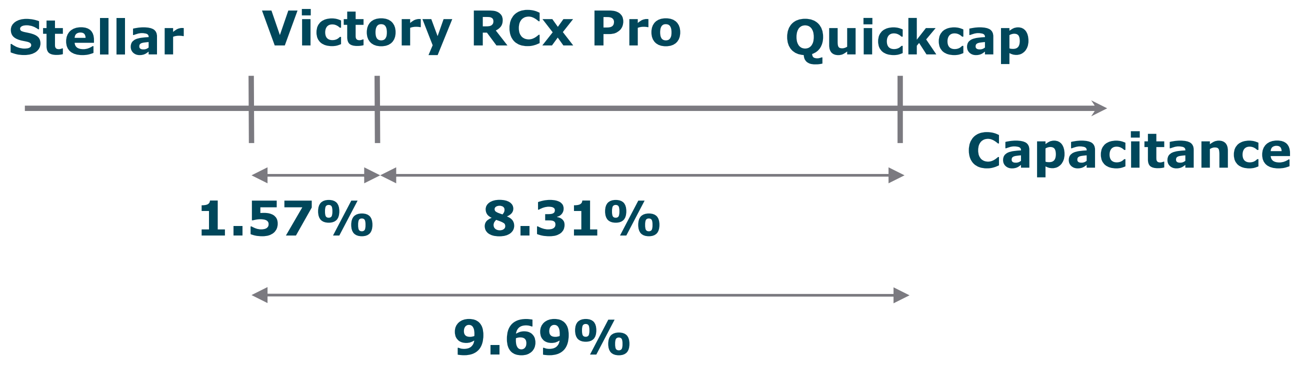


Stellar vs Victory RCx Pro



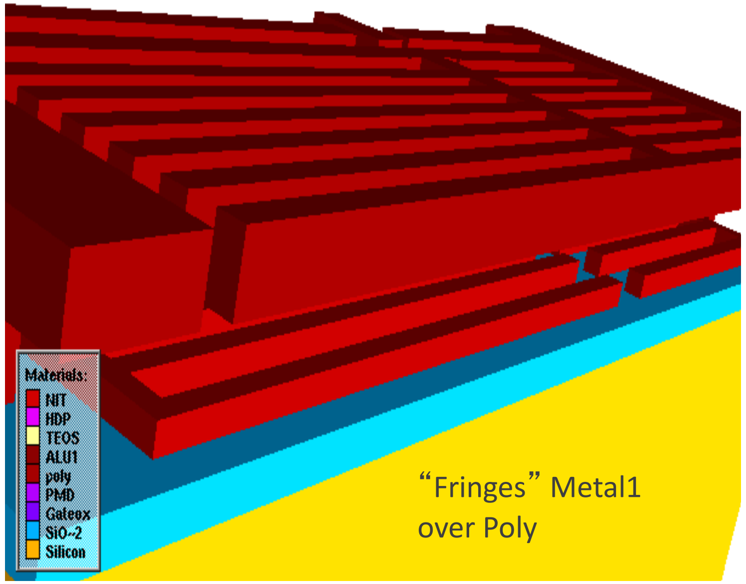
Capacitance Extraction on 83 Layouts

- Statistically capacitance values can be positioned in a diagram showing very good results consistency



Deep Submicron CMOS

- Three different ring oscillators



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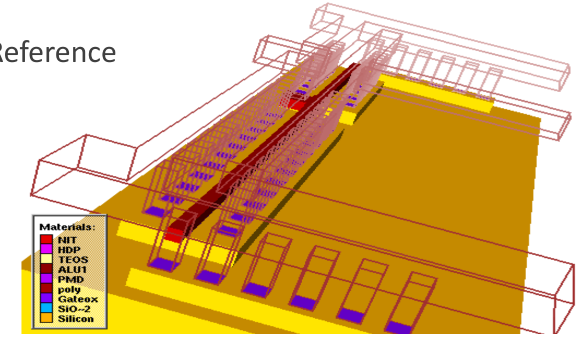
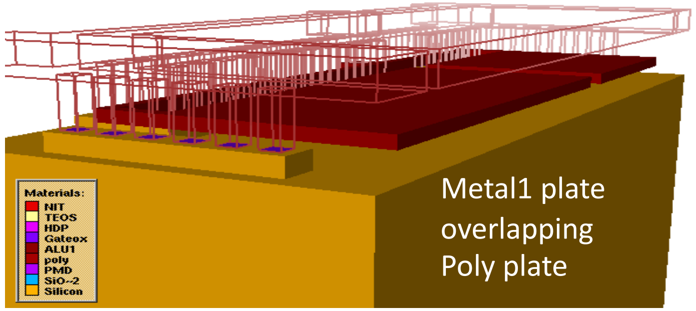
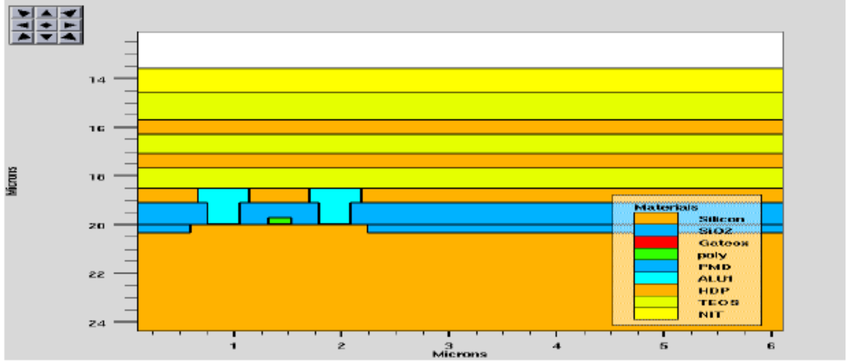




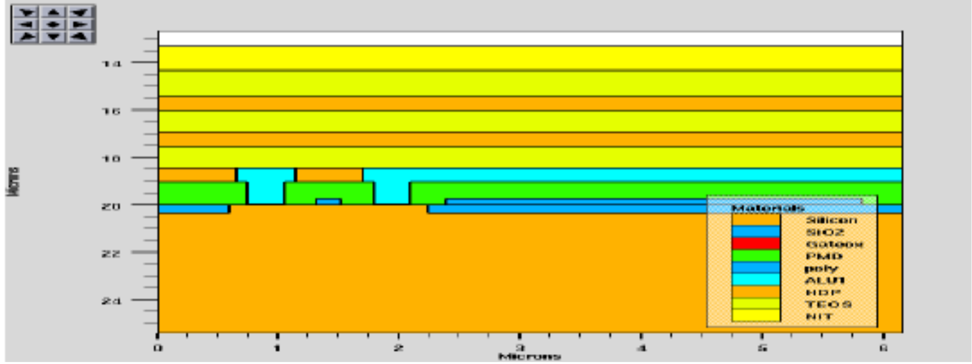
Deep Submicron CMOS

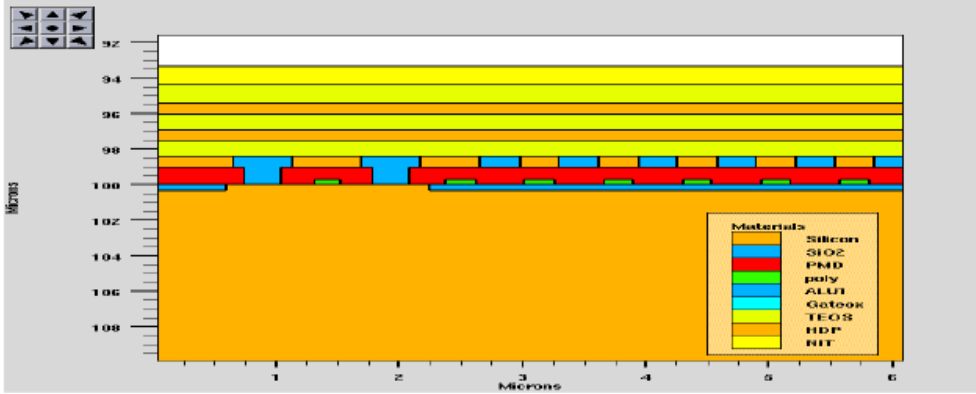
- 2D cutplanes of the different ring oscillator

Reference



Metal1 plate overlapping Poly plate





“Fringes” Metal1 over Poly

Deep Submicron CMOS

- SPICE simulation results
- Comparison with measurements

Reference

	Without RC	victoryrcx	diva	mes
Delay ps std	39.95	48.46	43	41
Delay ps wcs	39.95	48.39		

Metal1 plate overlapping Poly plate

	Without RC	victoryrcx	diva	mes
Delay ps std	39.95	62.98	65.4	61
Delay ps wcs	39.95	64.21		

“Fringes” Metal1 over Poly

	Without RC	victoryrcx	diva	mes
Delay ps std	39.95	59.60	79.5	57
Delay ps wcs	39.95	60.62		

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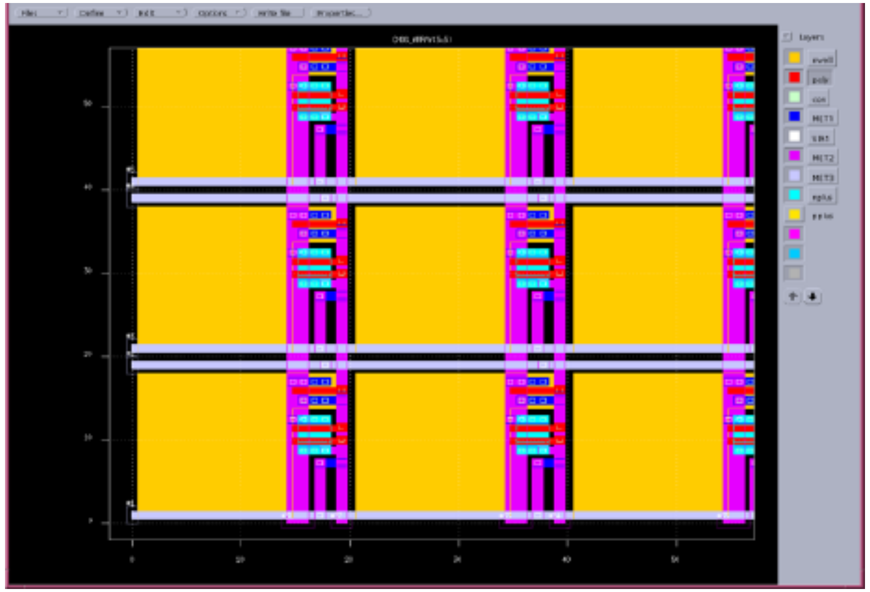
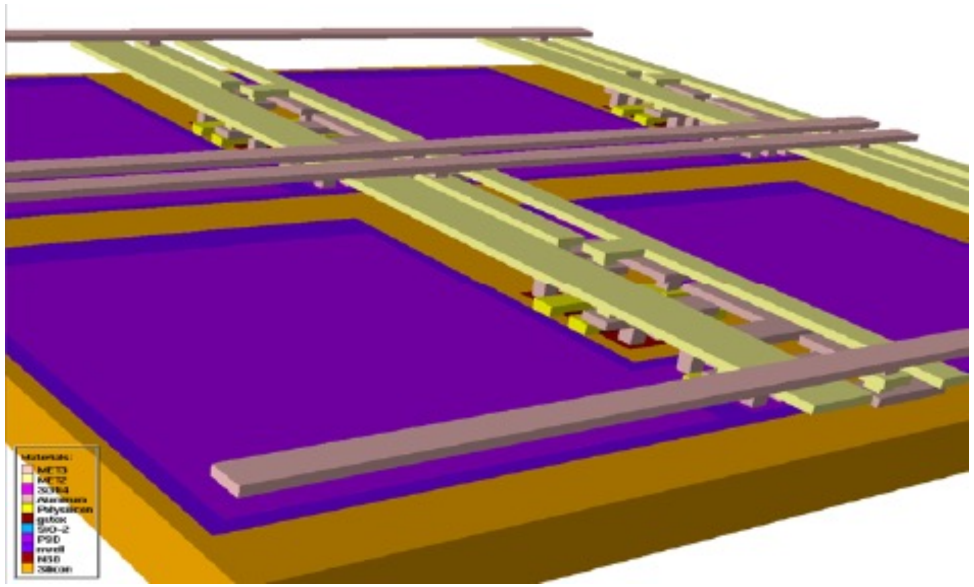
Deep Submicron CMOS

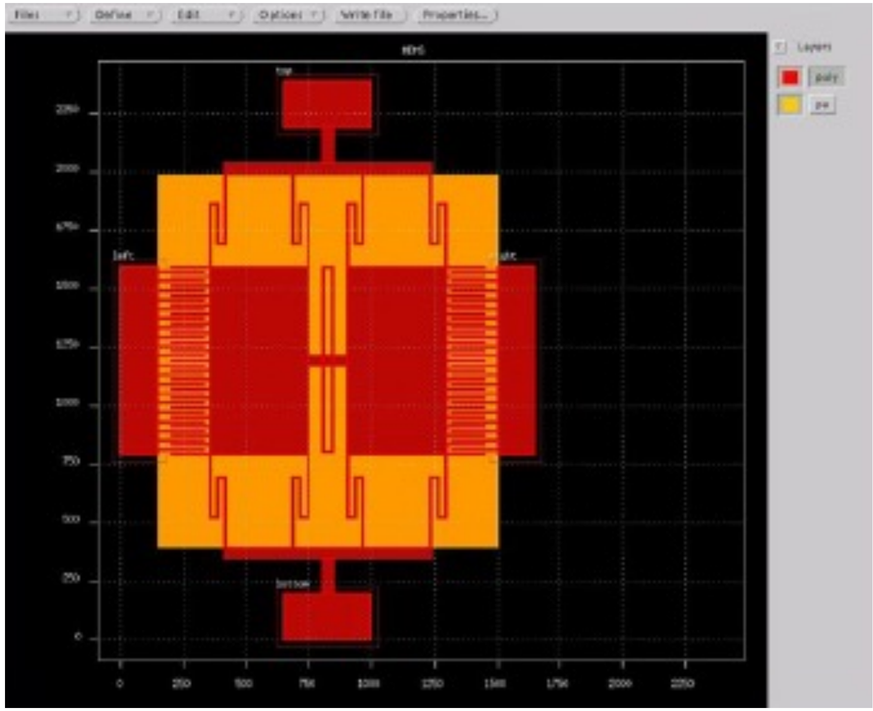
CMOS Sensor

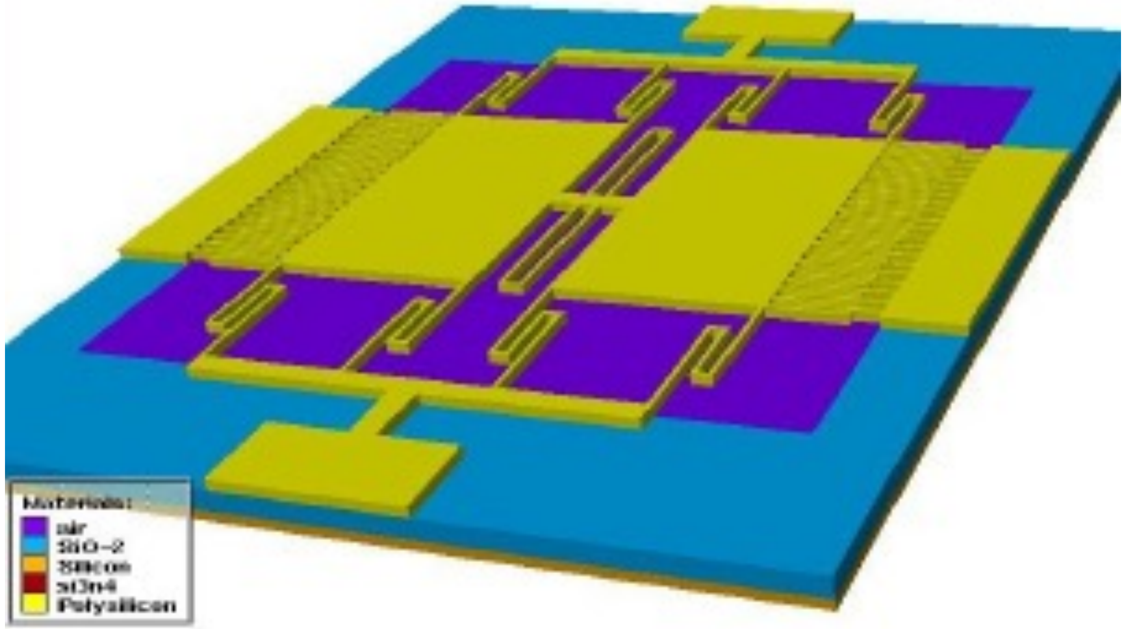




Deep Submicron CMOS

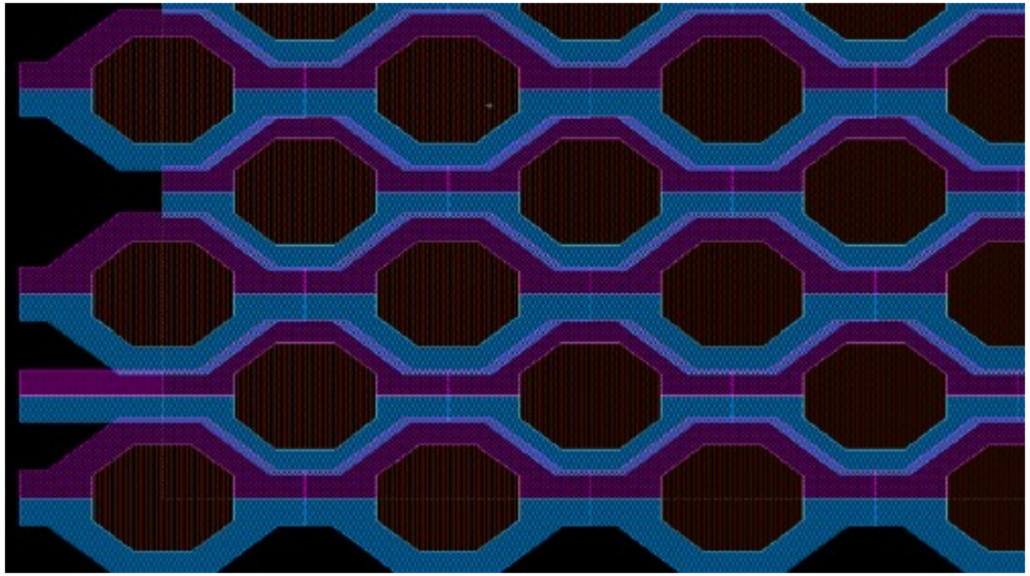
G Sensor

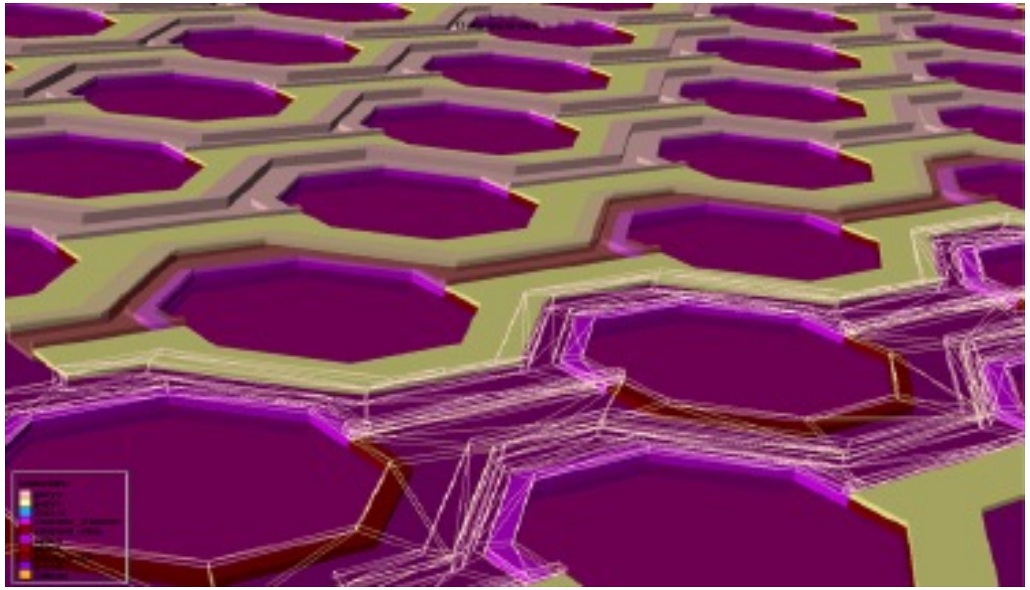




Deep Submicron CMOS

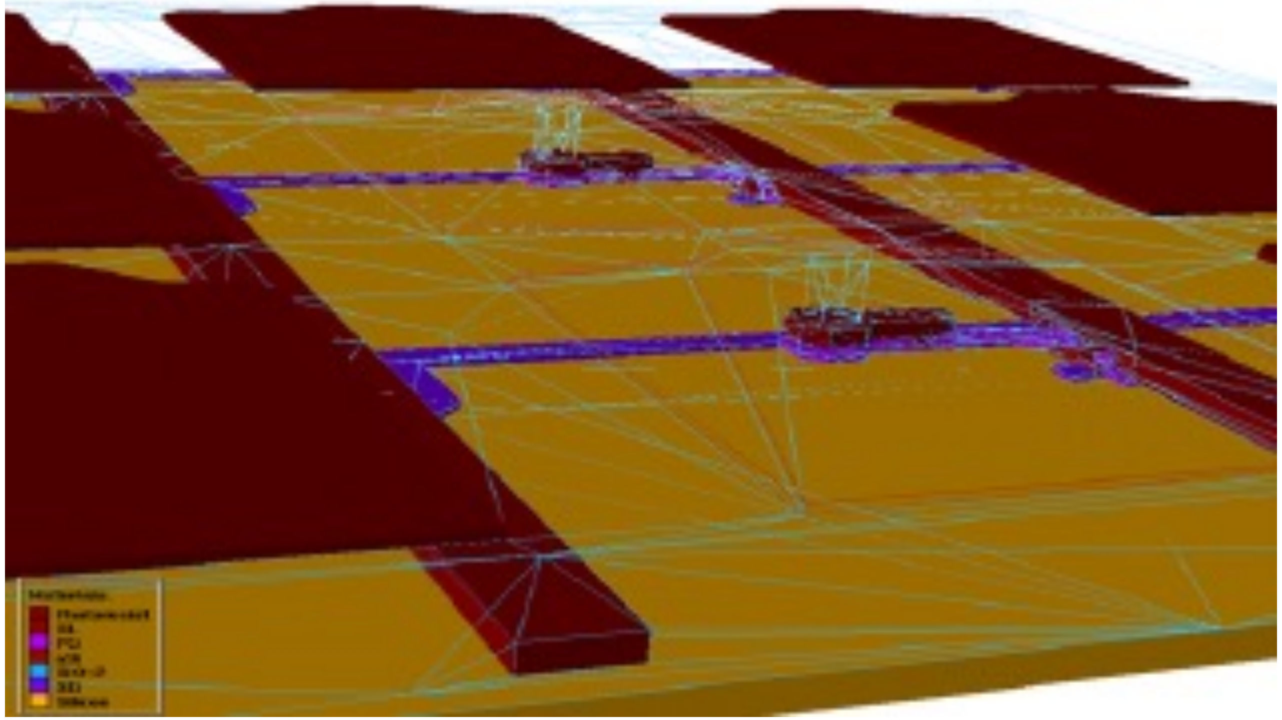
CCD Sensor Cell





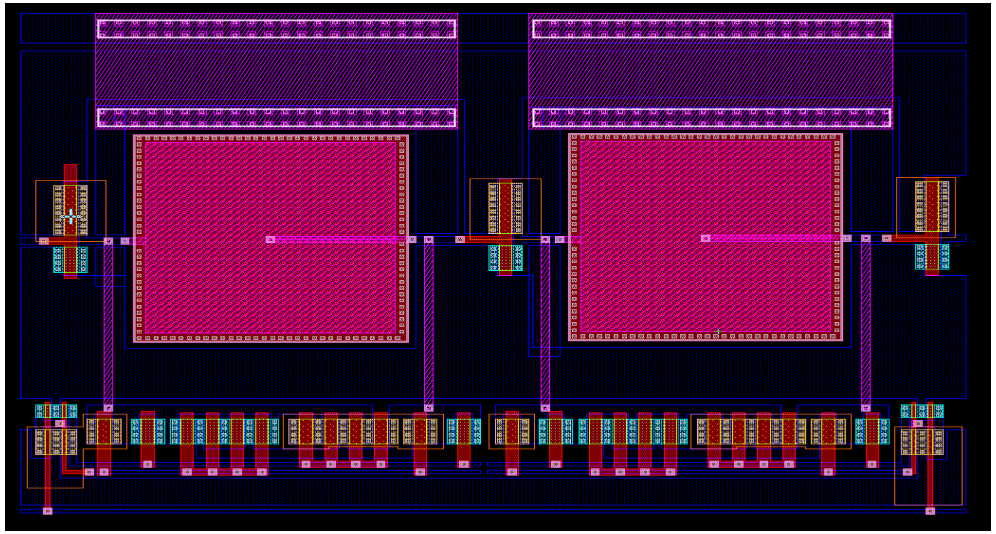
Flat Panel

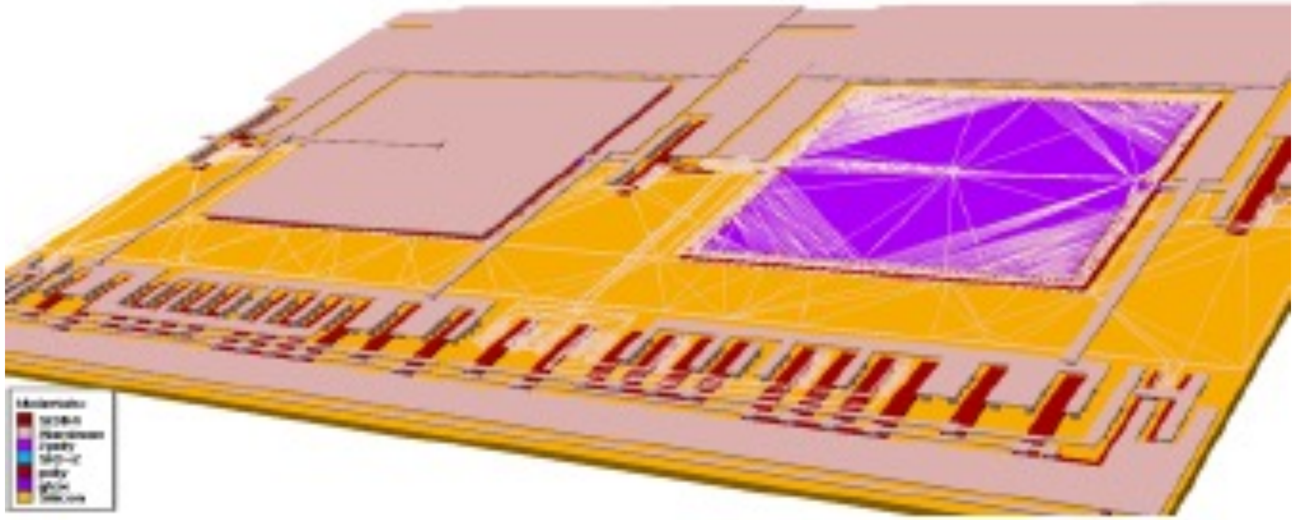
LCD/TFT Cell



Flat Panel

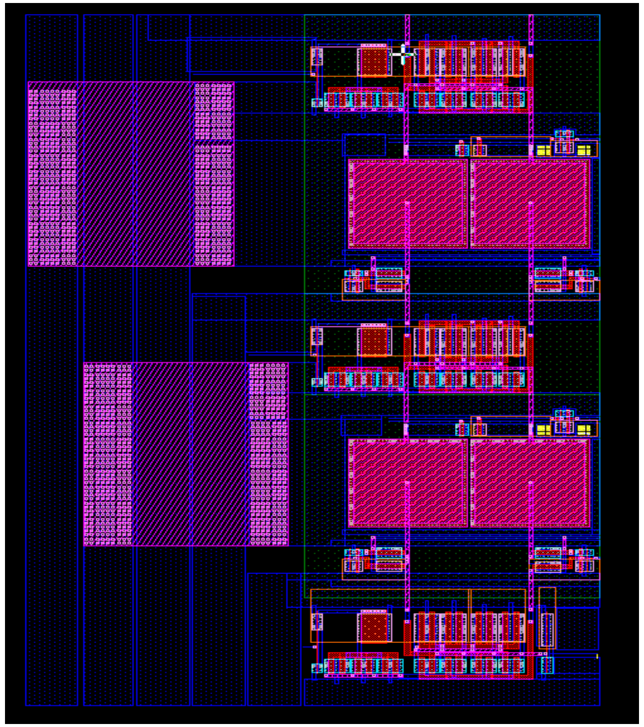
Comparator 1

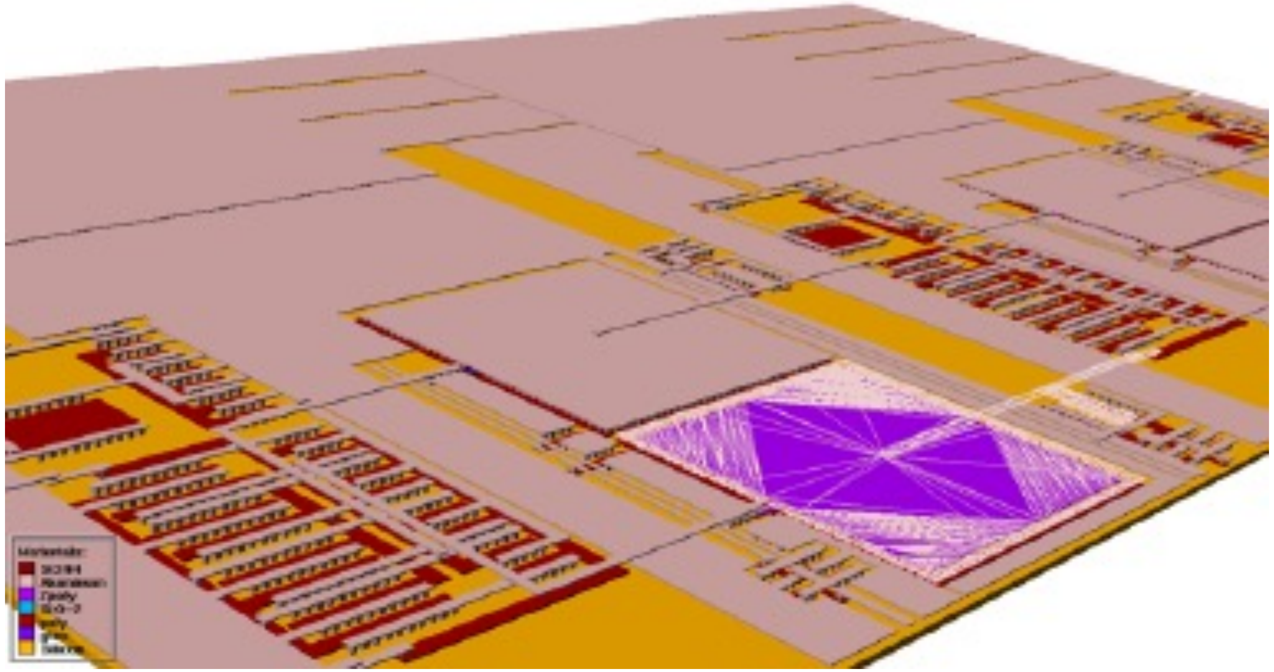




Flat Panel

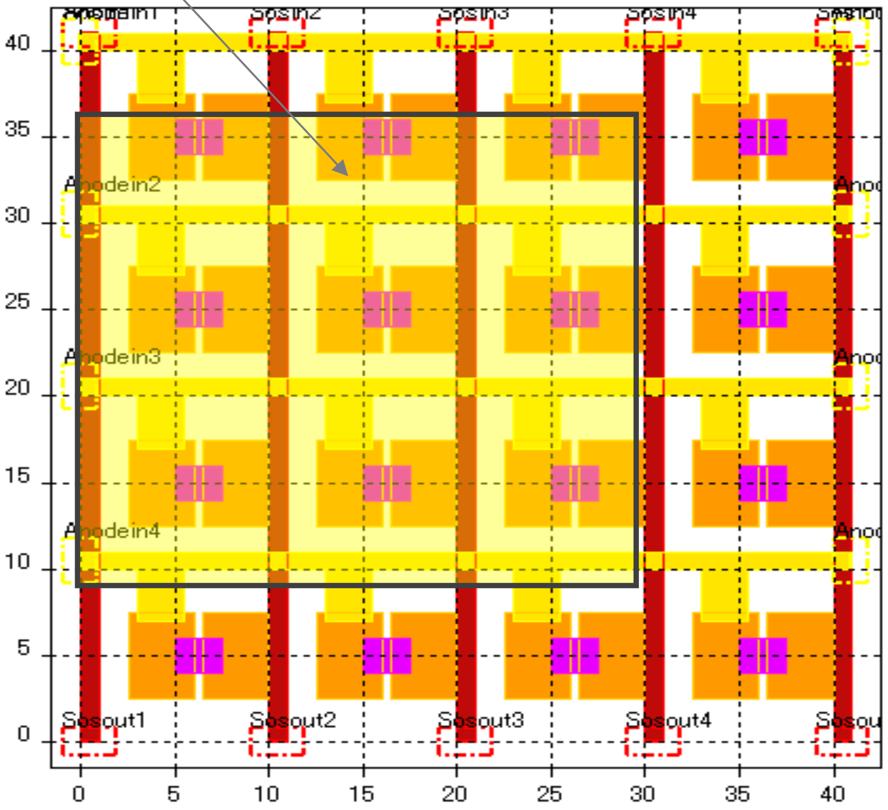
Comparator 2

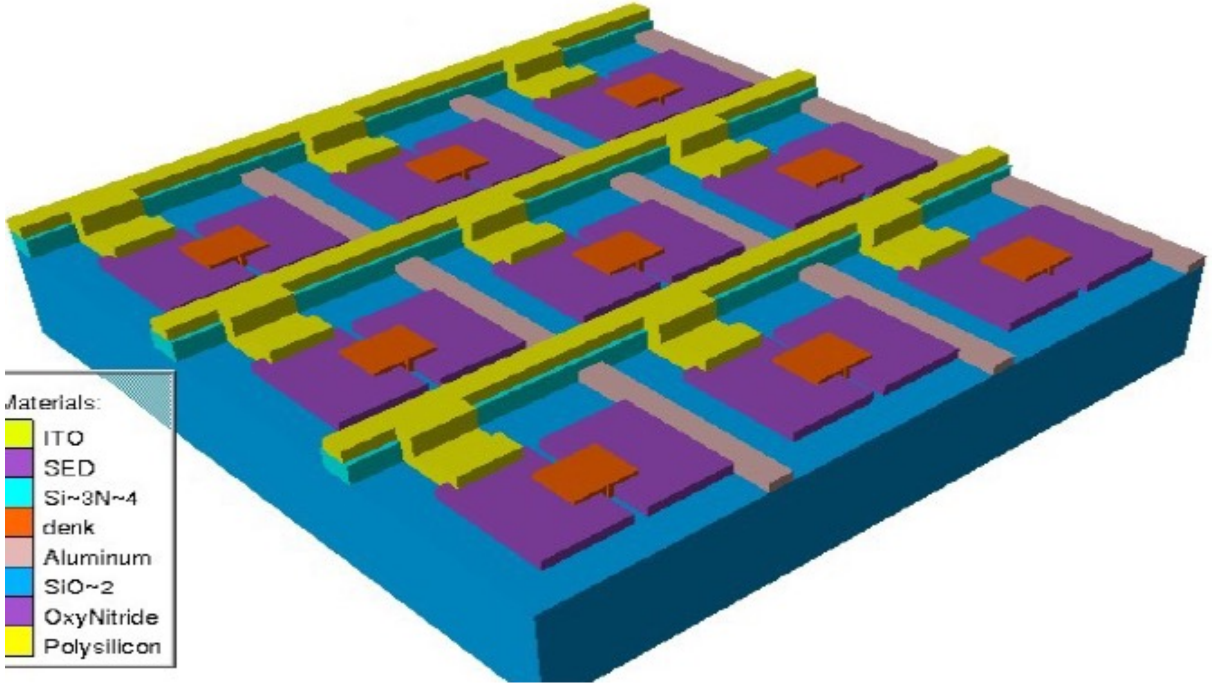




Flat Panel

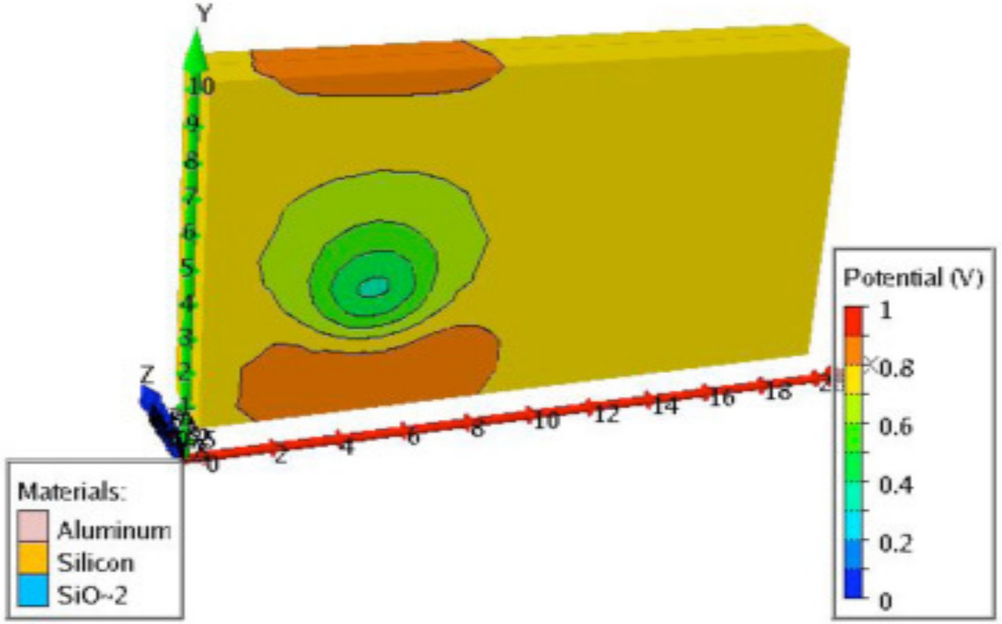
Simulation area (3x3 matrix)



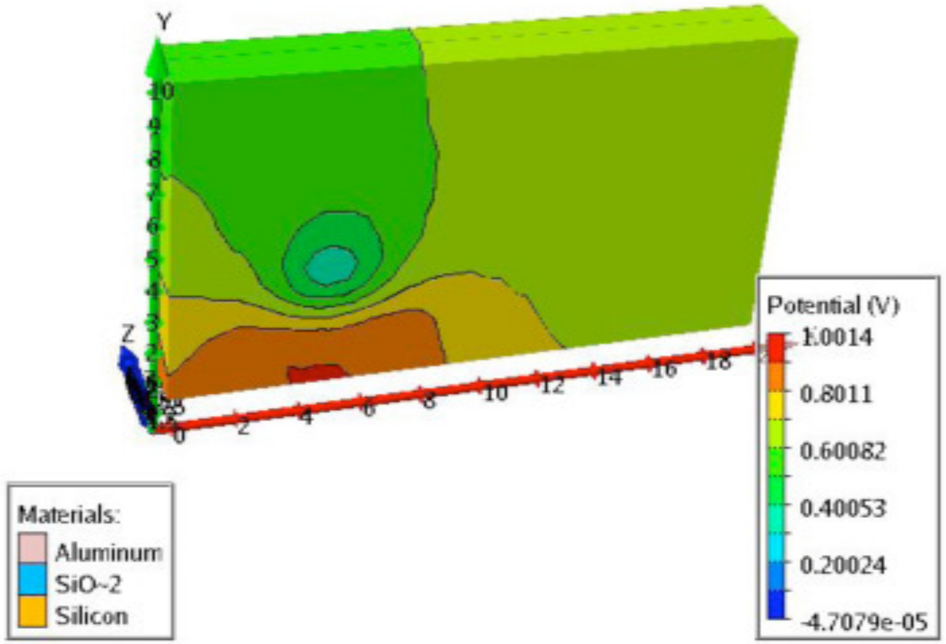


Flat Panel

Cyclic Boundary

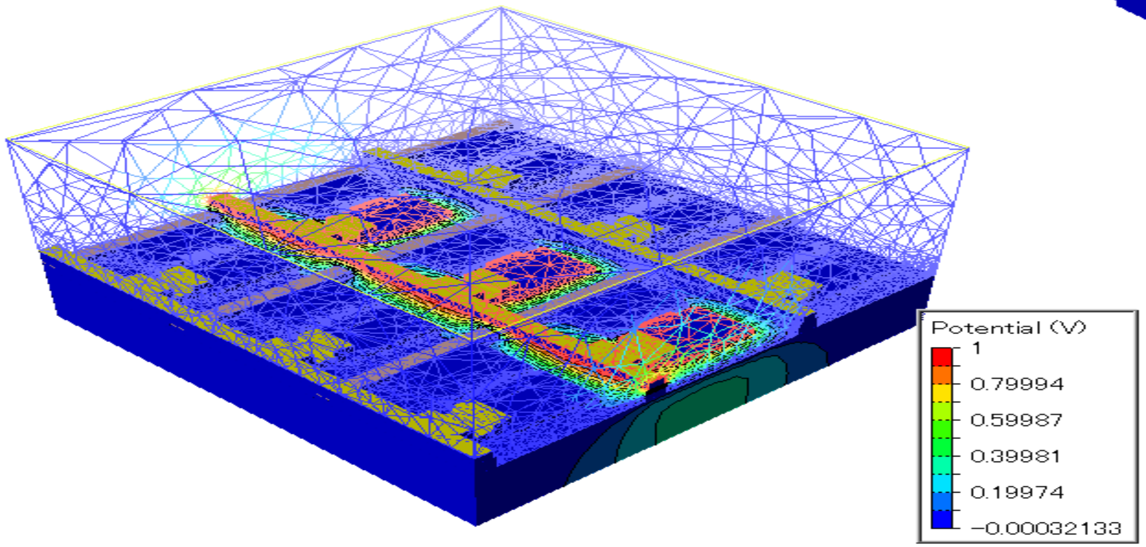


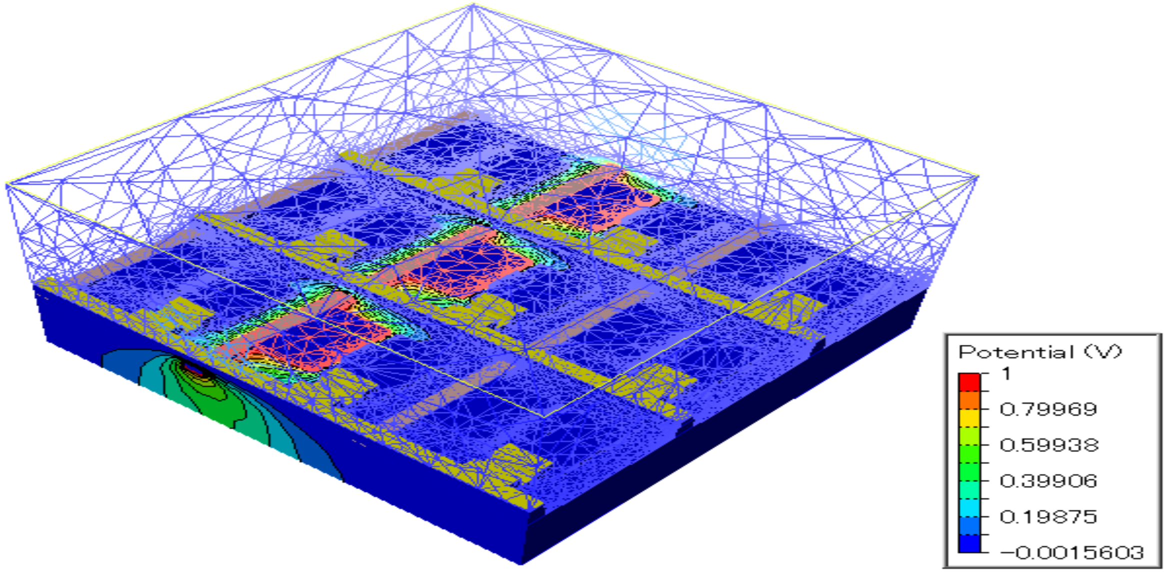
Mirror Boundary



Flat Panel

Potential apply to Gate2 Line

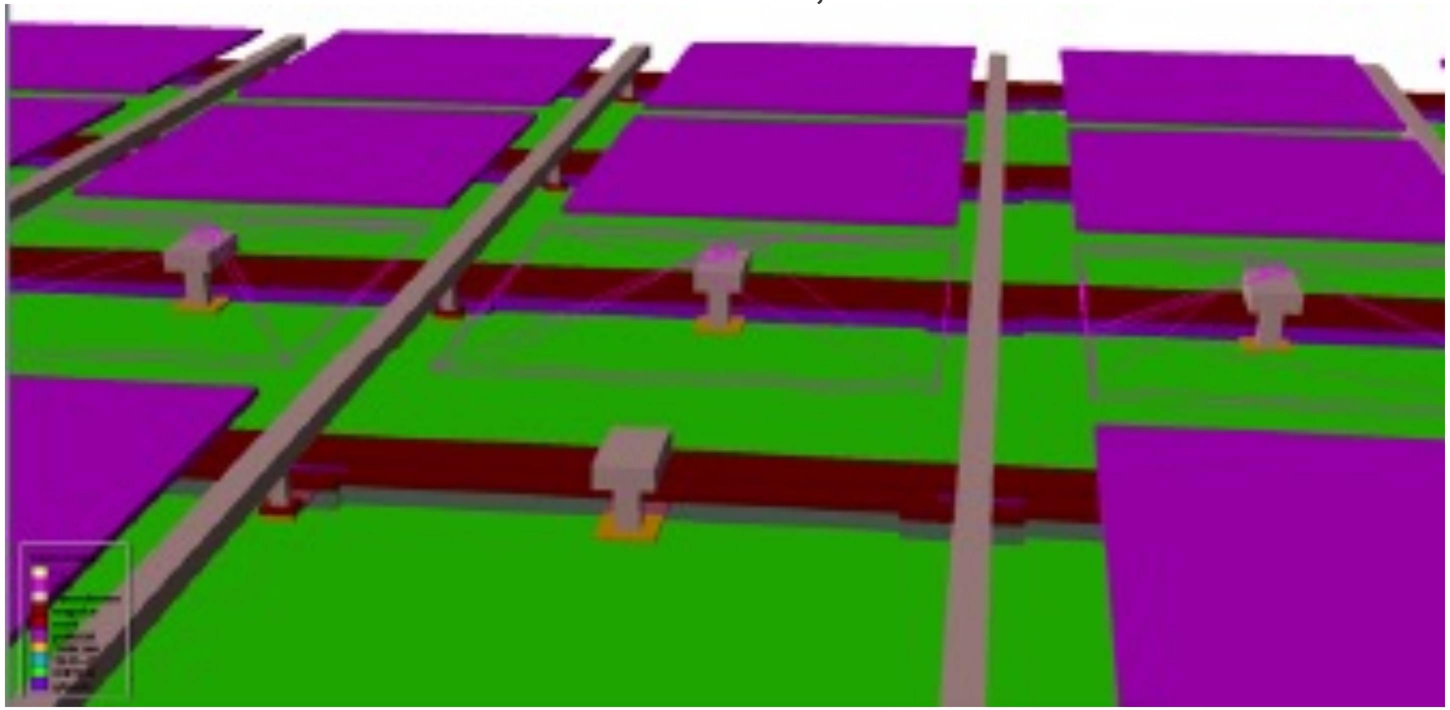


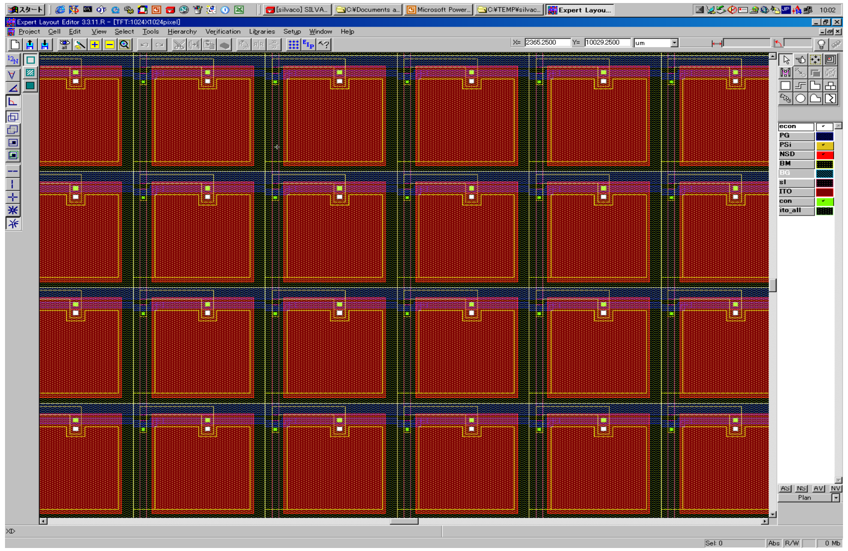


Potential apply to Sosin2 Line

Flat Panel

Flat Panel LCD, TFT

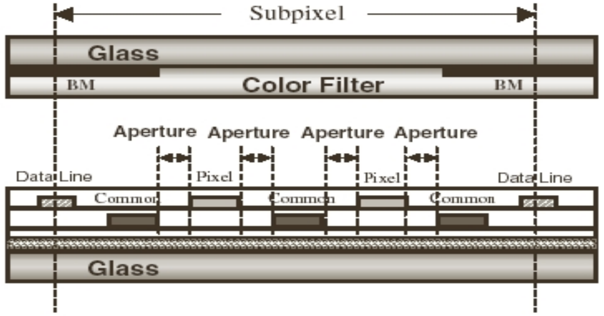


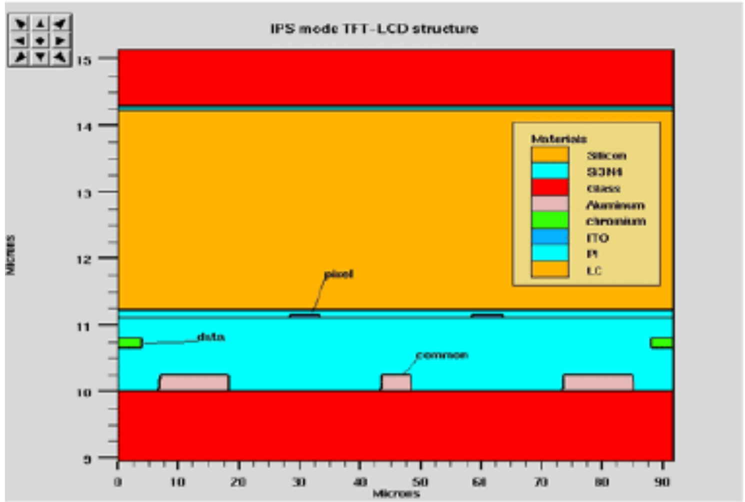


Flat Panel

AMLCD-TFT BMT:

Coupling Capacitance

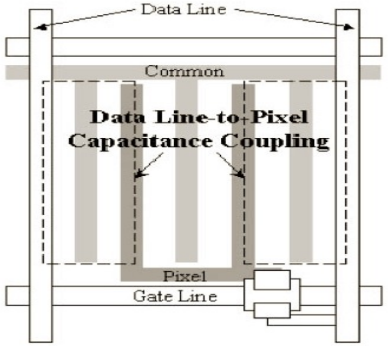


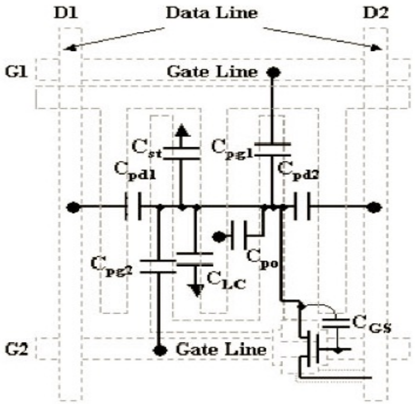


	Clc (Victory RCx Pro)	Cdc (Victory RCx Pro)	Clc+Cdc (Victory RCx Pro)	Clc+Cdc (Victory RCx Pro)
pixel_0	42.2	61.0	103.2	99.60
pixel_1	32.8	61.1	93.9	93.46
pixel_2	31.6	58.8	90.4	91.25

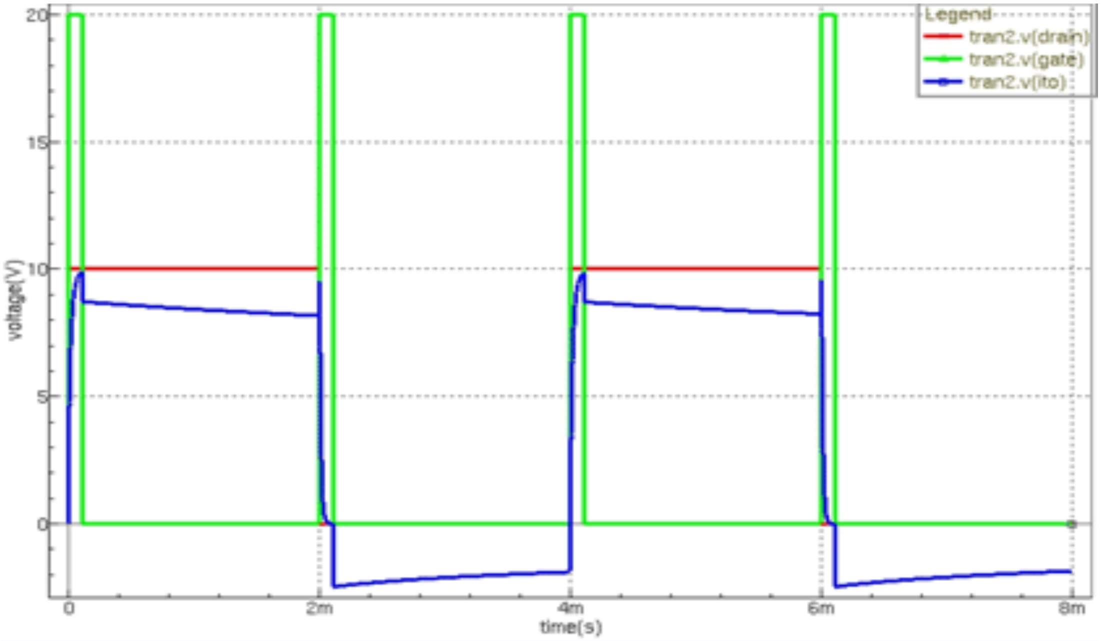
Flat Panel

AMLCD-TFT BMT:



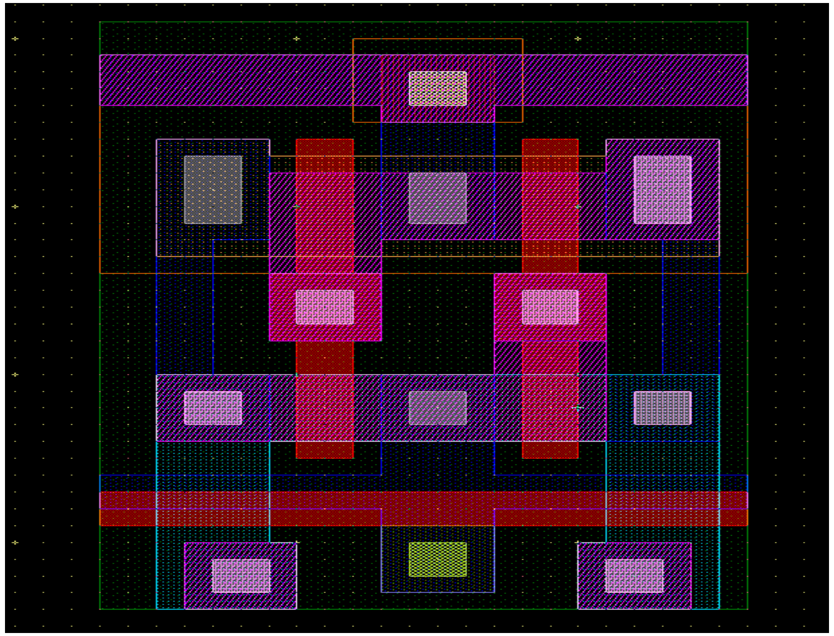


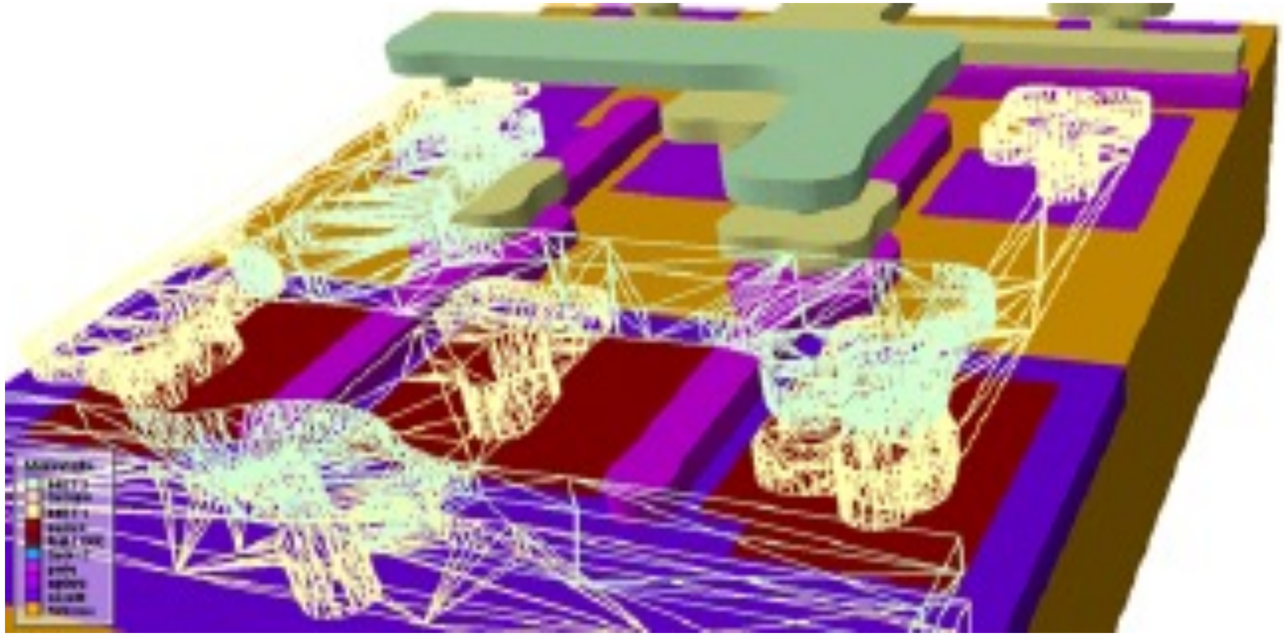
RC delay effect across data line on one Pixel



Memory Cells

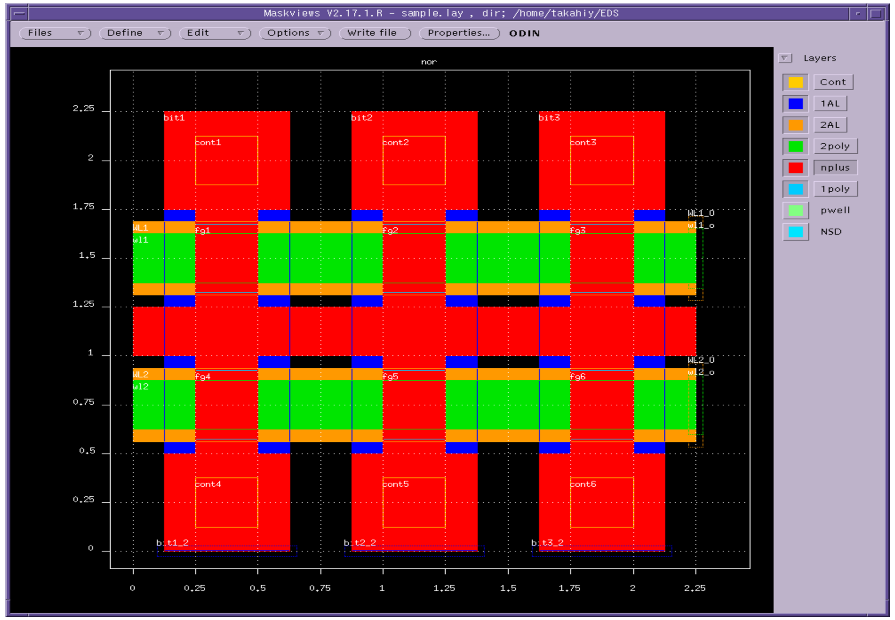
SRAM CELL

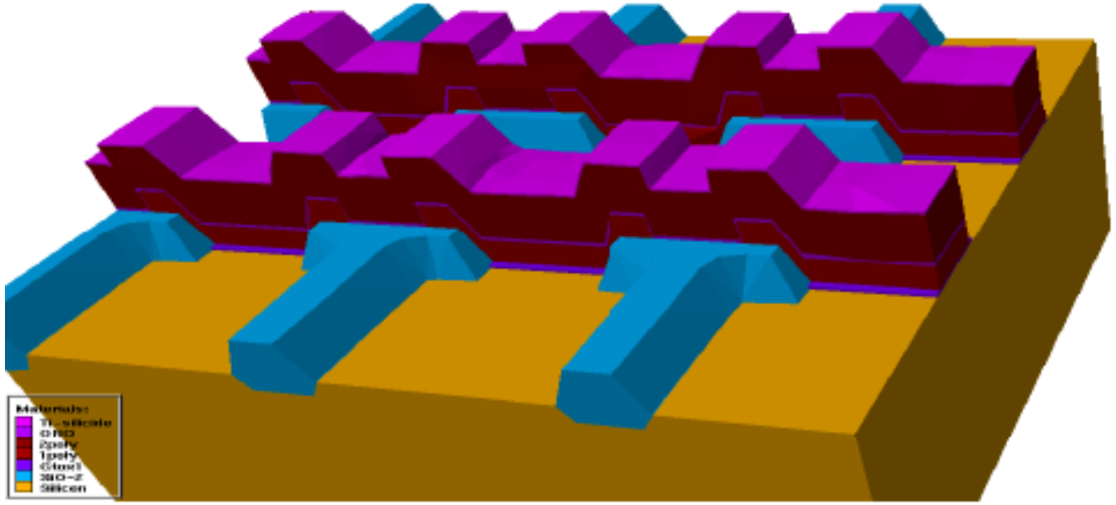




Memory Cells

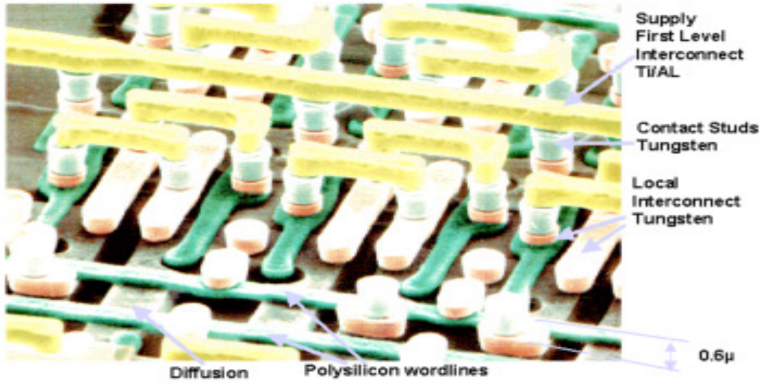
Flash Memory: NOR



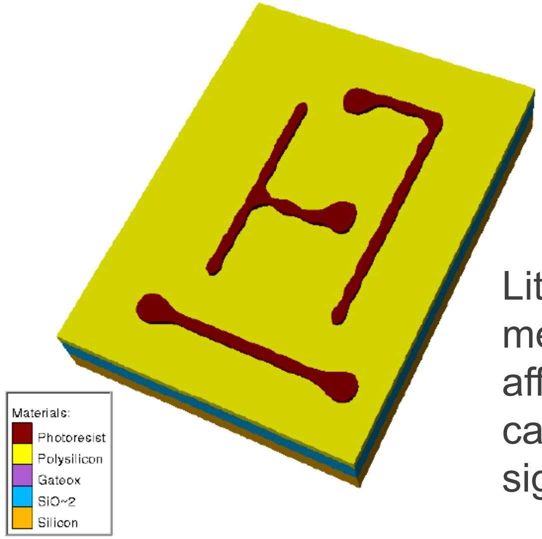


Memory Cells

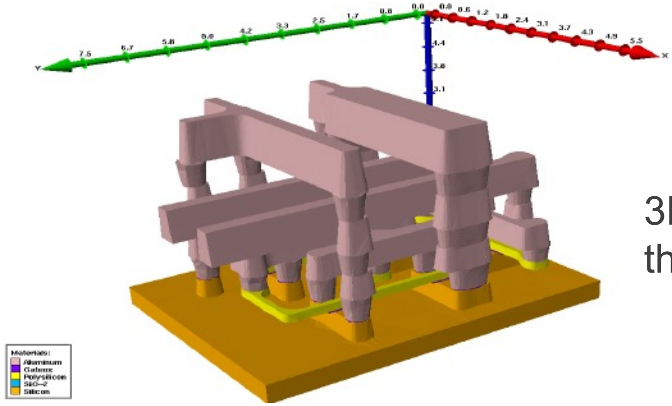
- SRAM and Flash memory cell
- Victory RCx uses advanced 3D process simulation to convert SRAM layout into an accurate 3D representation of the SRAM cell
- Electrical field solutions on the realistic 3D geometry allow accurate extraction of parasitics



Six memory cells of partially completed SRAM array after removal of oxide insulation.
SEM photograph (IBM)



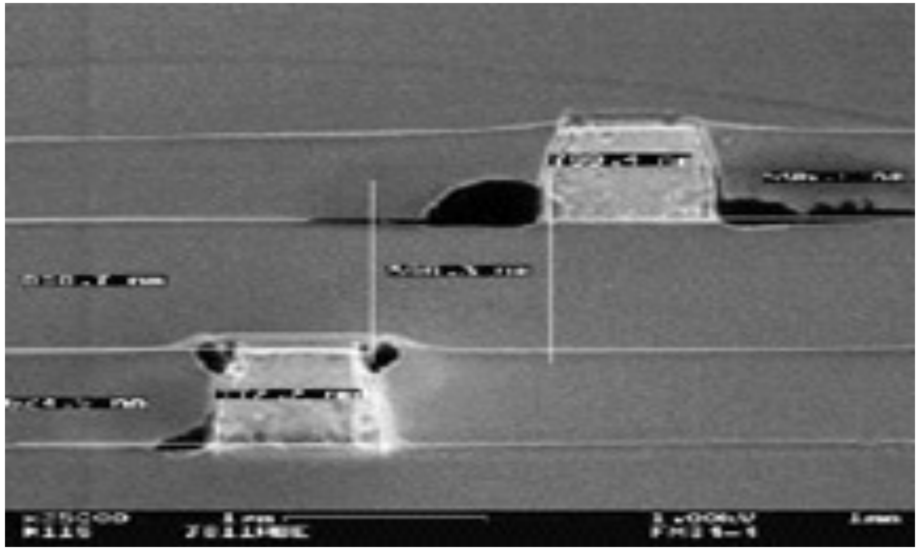
Lithographic effects on metal geometry can affect the resulting capacitance significantly.

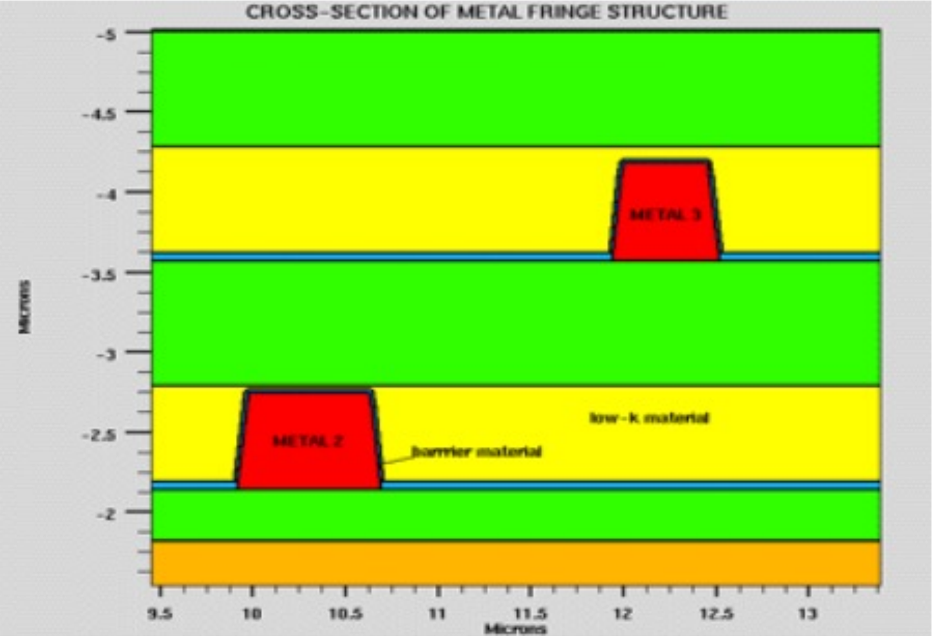


3D structure of the SRAM

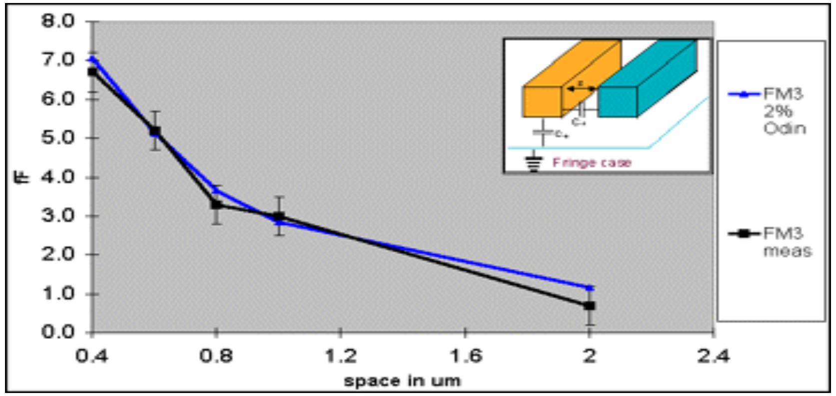
Memory Cells

- SEM photography of 2D sectional area
- Cross-section of metal fringe structure

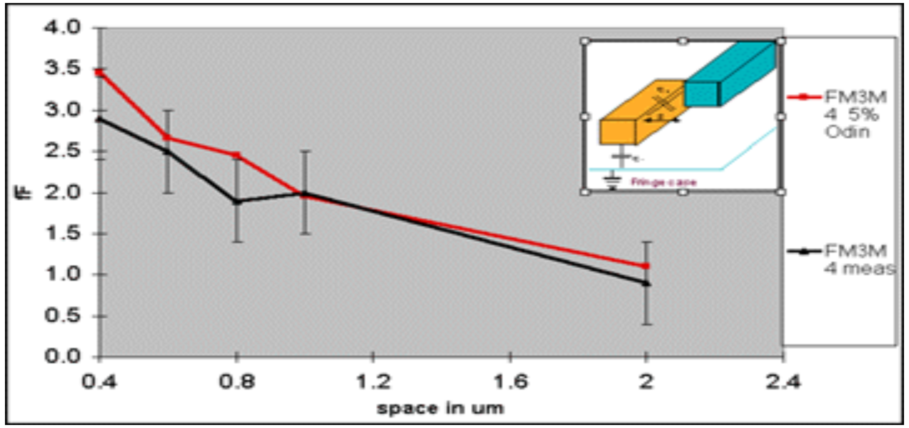




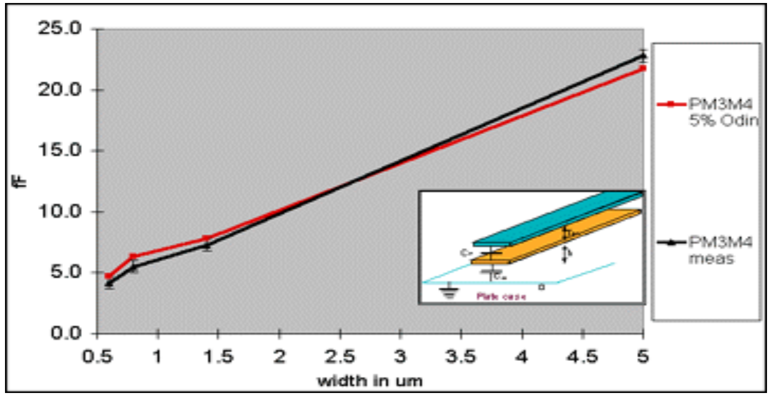
Memory Cells



Comparison between simulation (▲) and measurements (■) for lateral capacitance. Two parallel lines of metal 3 of 0.6um width and 100 um length.



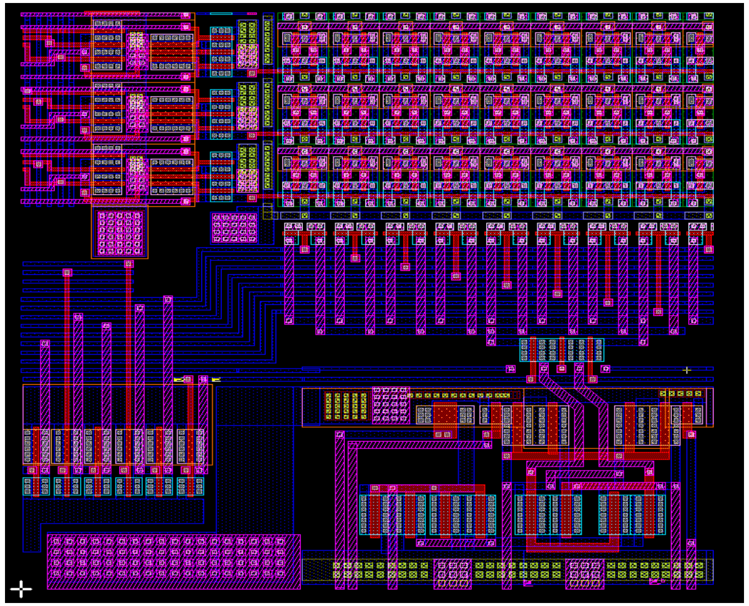
Comparison between simulation (■) and measurements (▲) or different layer fringe or edge capacitance. Two parallel lines of 0.6um width and 100 um length with one line in metal 3 and the other of metal 4.

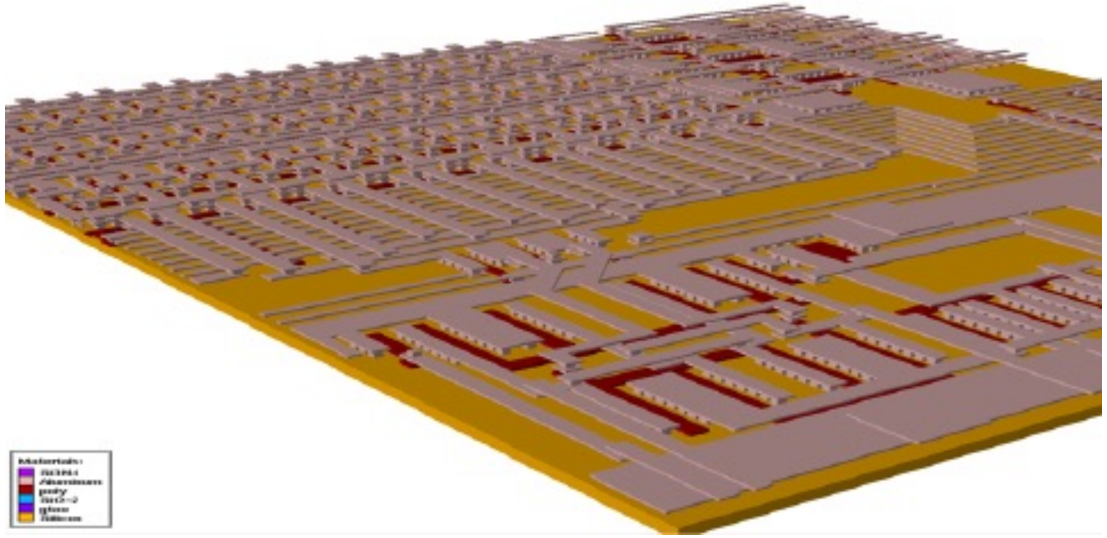


Comparison between simulation (■) and measurements (▲) for two stacked lines. Two parallel lines of metal 3 and metal 4 without any overhang.

Memory Cells

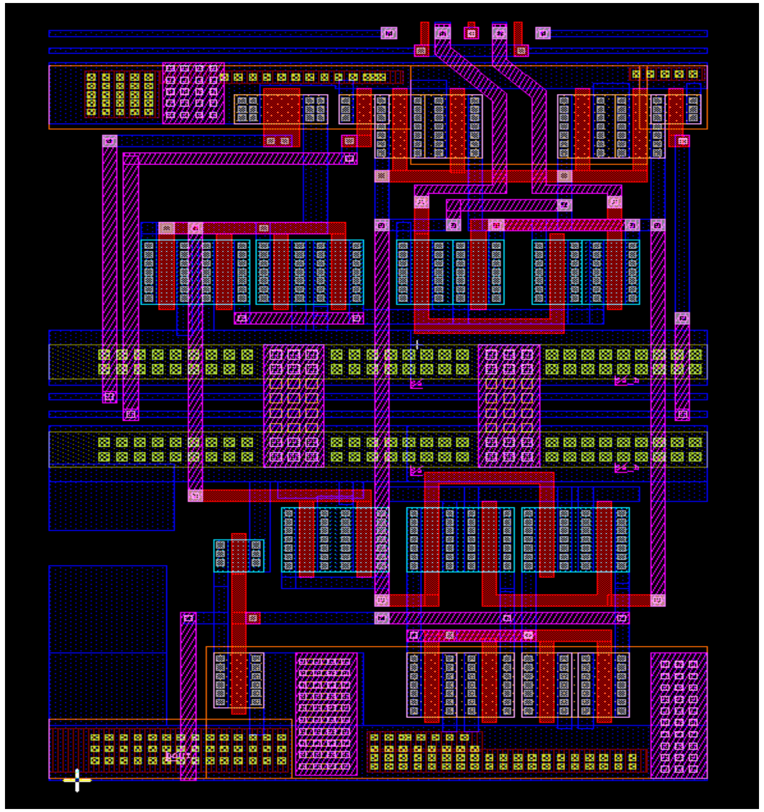
SRAM CELL and Decoder, Sense AMP

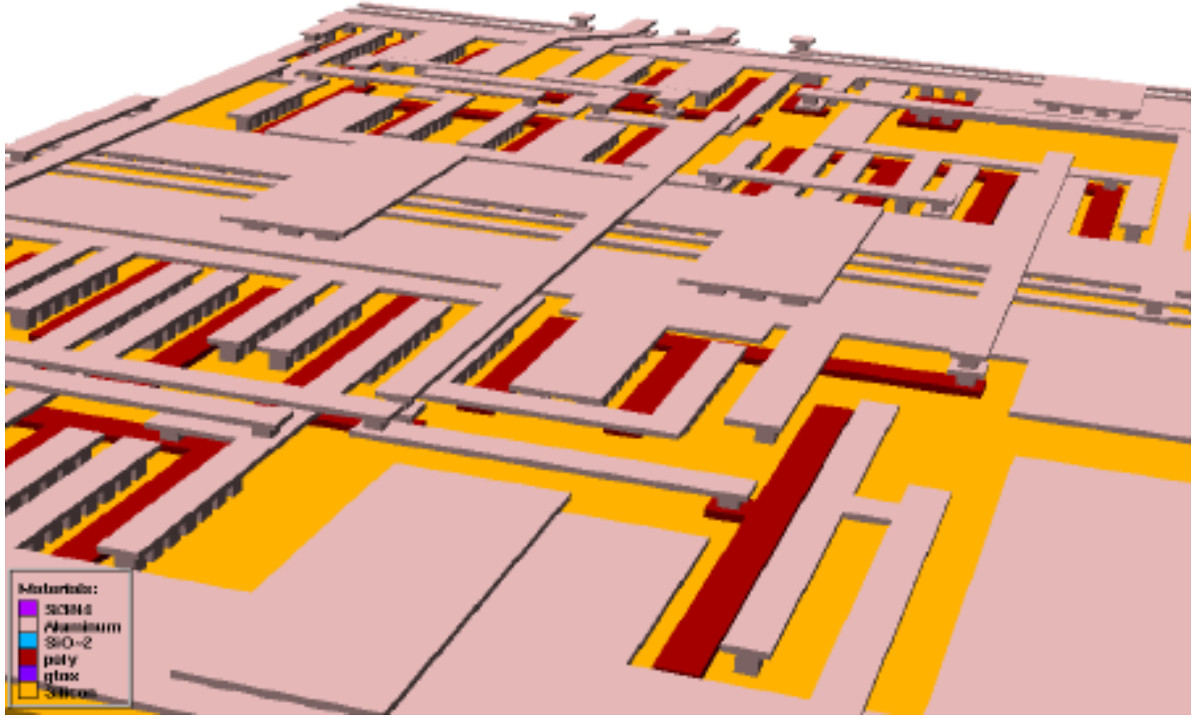




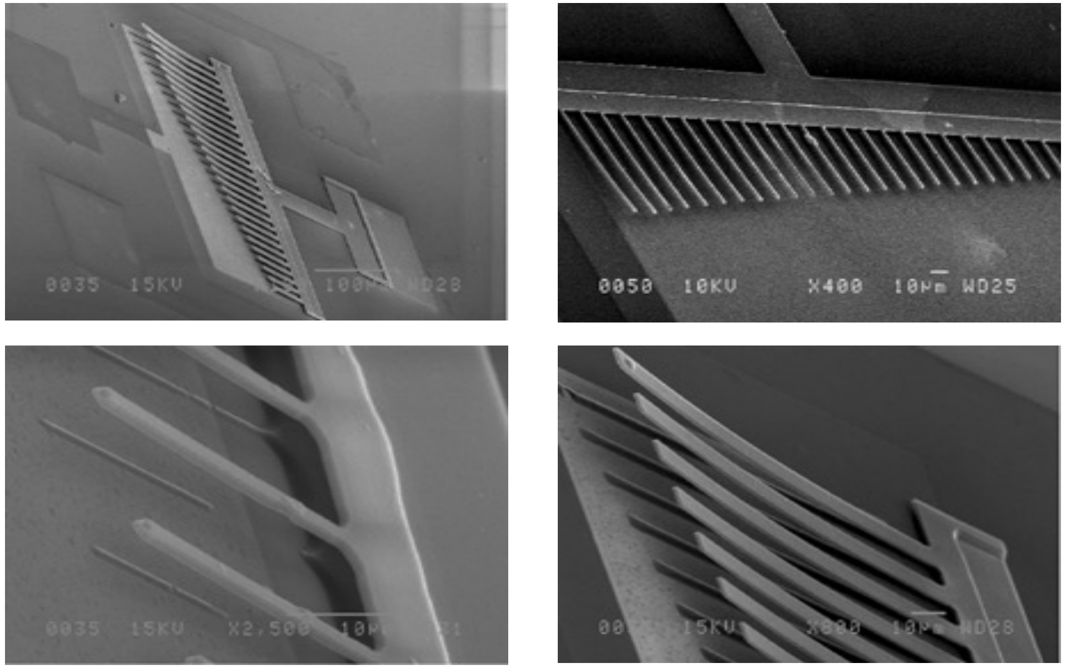
Memory Cells

Sense AMP



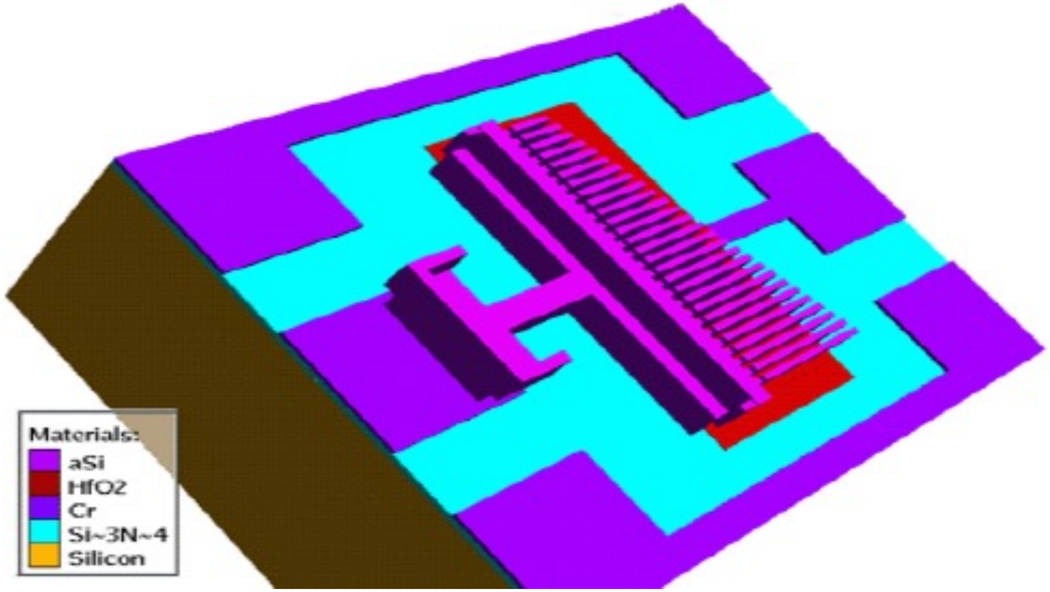


MEMS Simulation



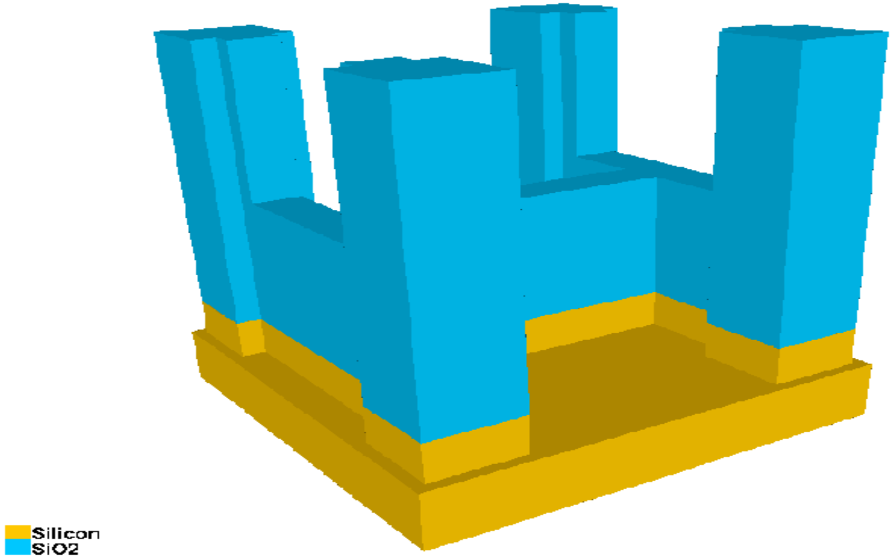
SEM morphologies of the fabricated capacitors with different width and lengths

Results from 3D simulation of the MEMS process flow using Victory RCx Pro

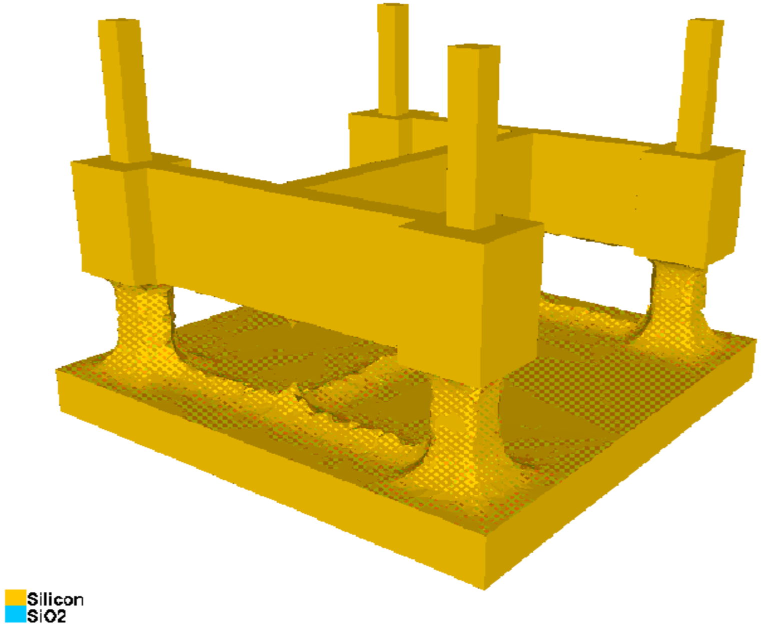


MEMS Simulation

A partial creation of an electrostatic MEMS



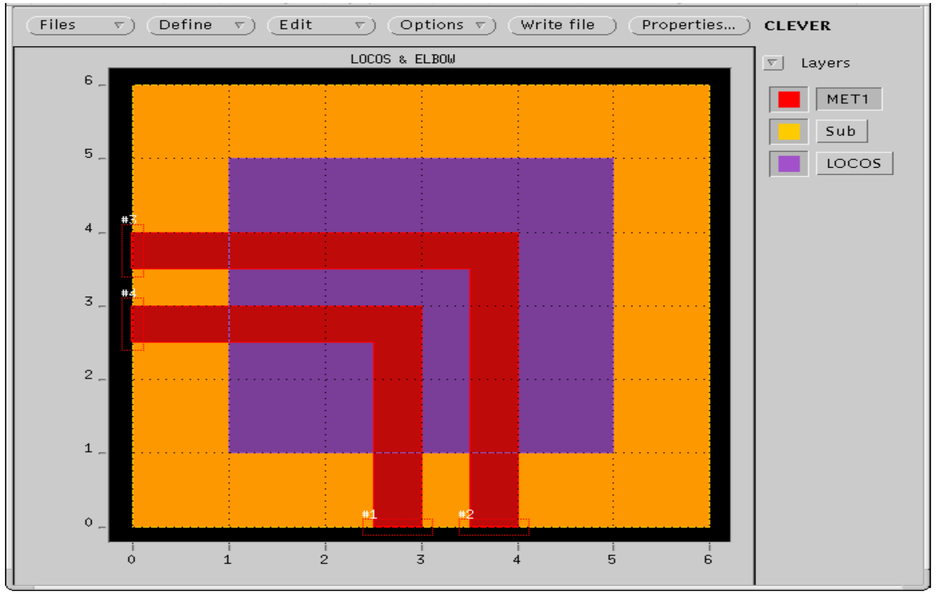
Part of a MEMS actuator array.



MEMS device after isotropic release etch.

Local Interconnect

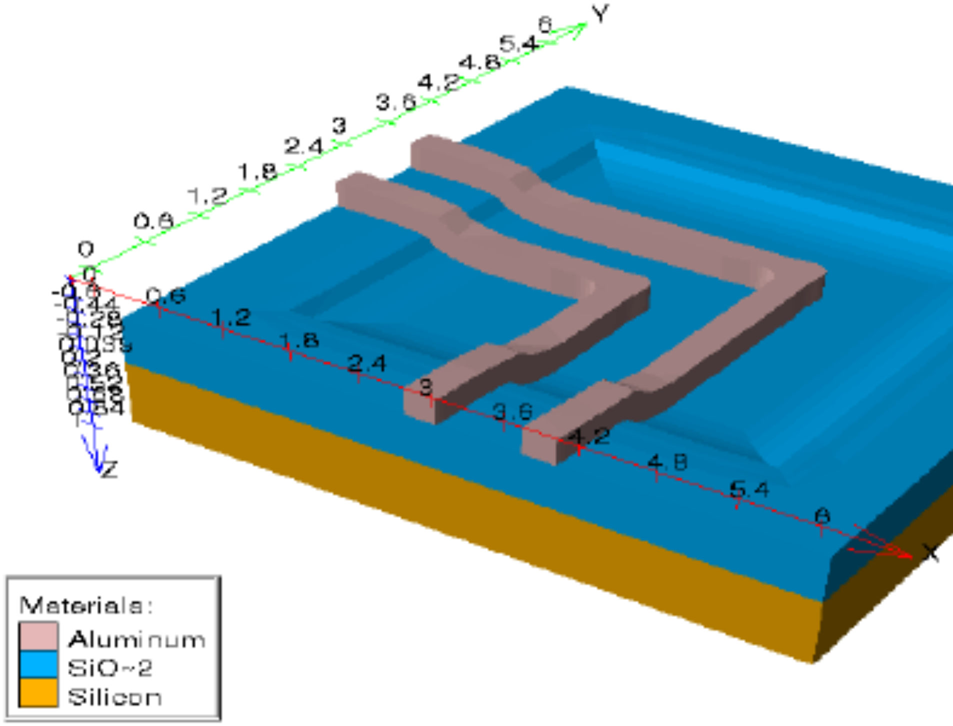
Victory RCx Pro Non-planar pattern:



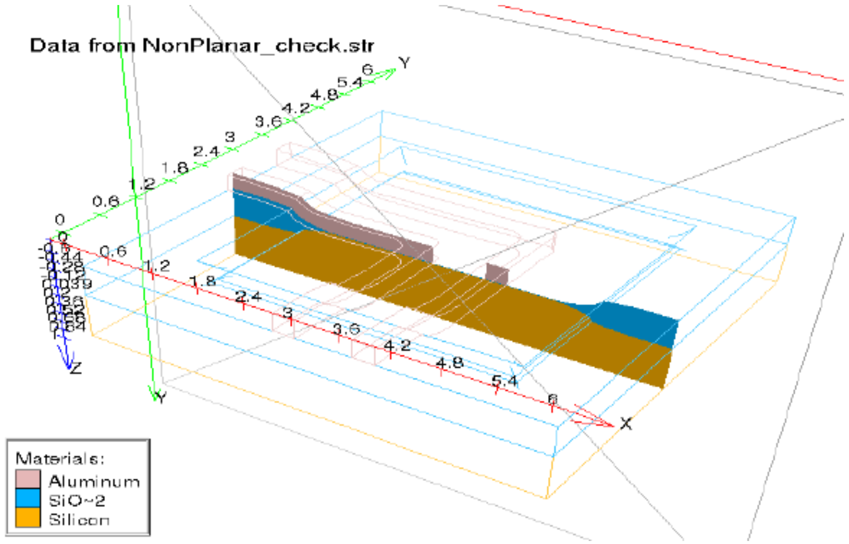
TEST Pattern

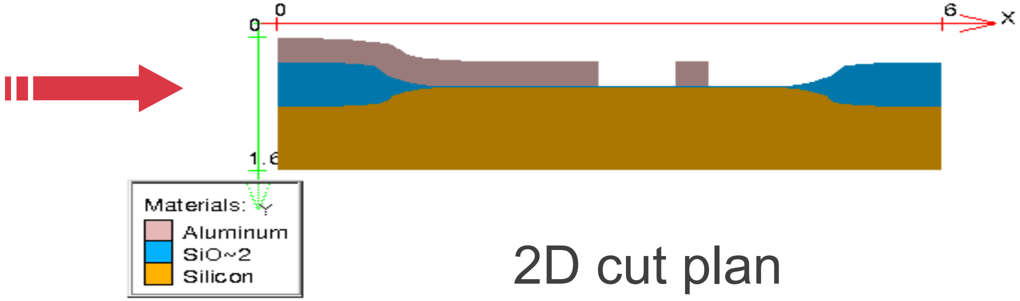
Default Materials Parameter		
Material Name	Relative Permittivity	Conductivity [A/V cm]
Aluminum		376676
BPSG	3.9	
BSG	3.9	
Copper		588235
Material(“string”)	3.9	
Oxide	3.9	
OxyNitride	7.5	
Nitride	7.5	
Resist	3.9	
Polysilicon		376676
Silicon	3.9	
TEOS	3.9	
Tungsten		200000

Local Interconnect



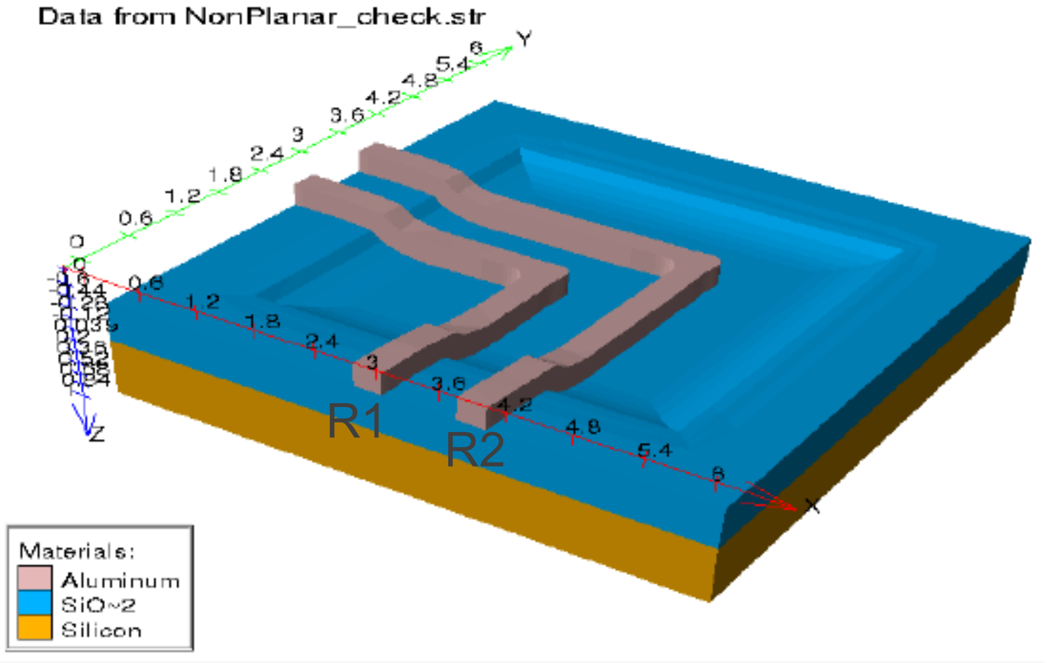
3D structure





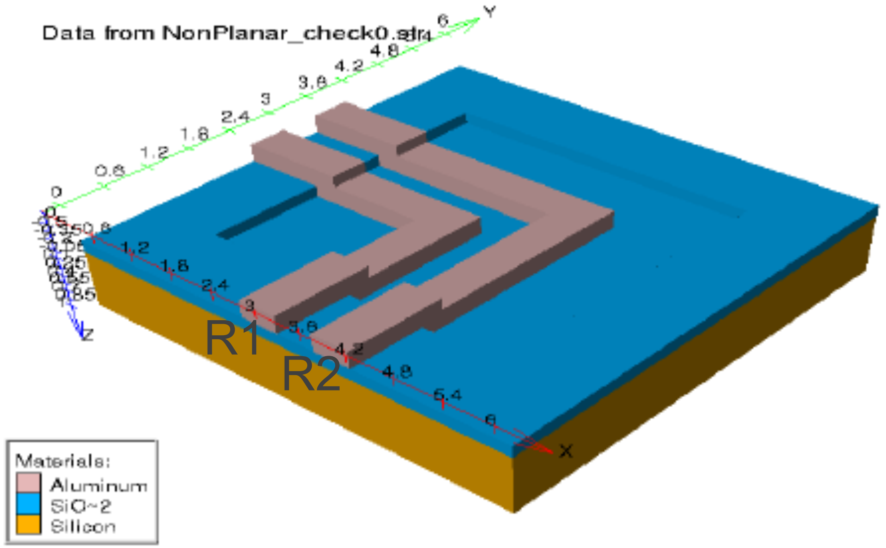
2D cut plan

Local Interconnect



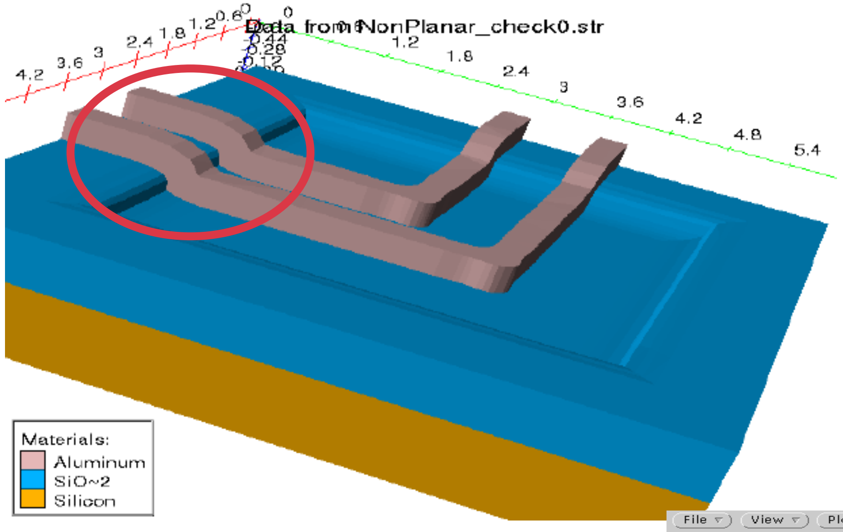
LOCOS+Litho Physical Process

	Physical	Geometrical
R1	1.6319044	0.9288782
R2	2.2651981	1.2825422

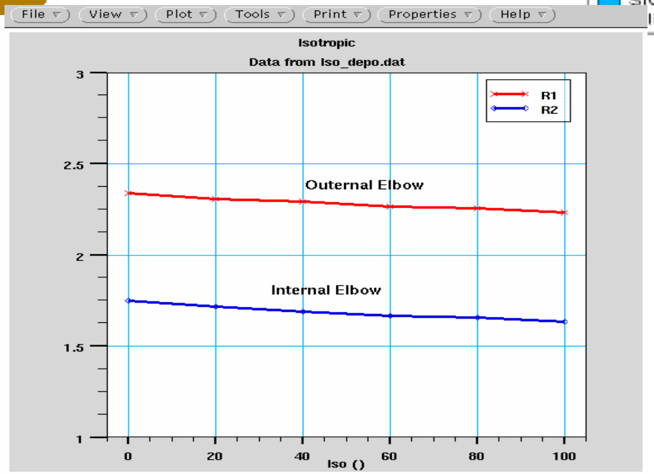


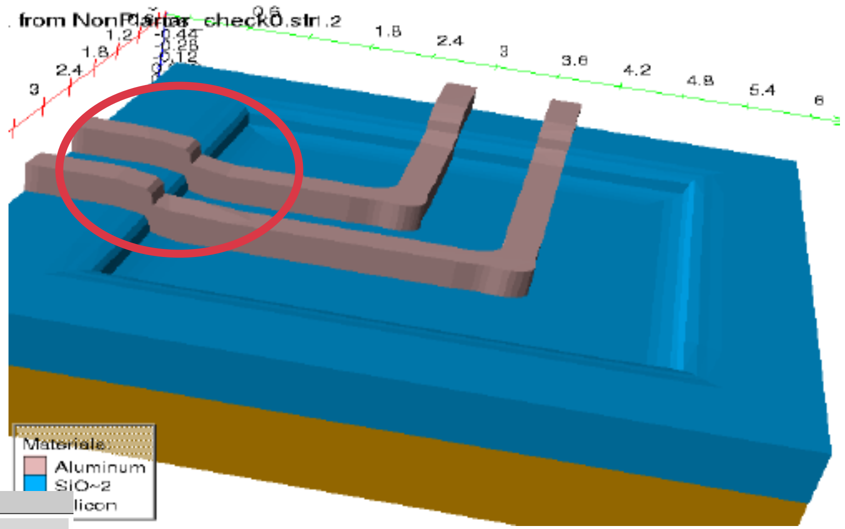
Step Etch + no Litho Geometrical

Local Interconnect



Isotropic 1

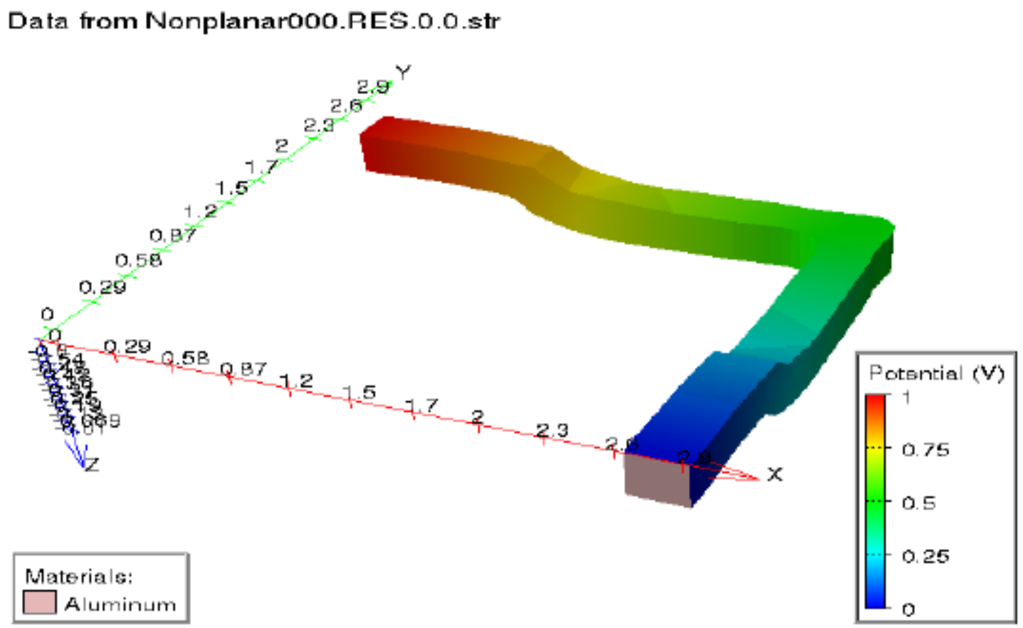




Isotropic 0

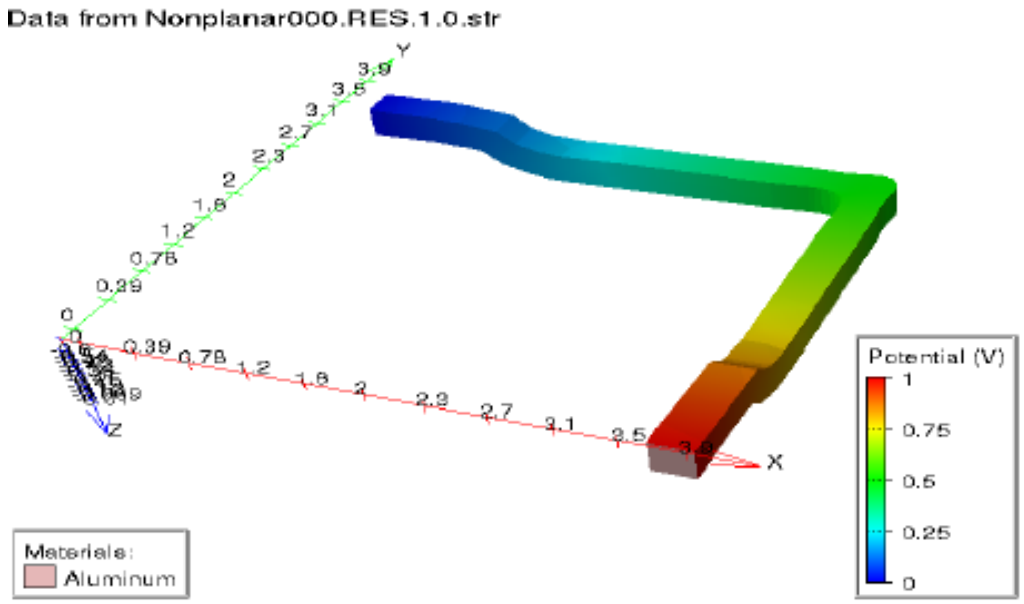
Local Interconnect

Internal elbow electric field



R=1.6319044

External elbow electric field



R=2.2651981

Conclusions

- Victory RCx should be used for parasitic RC extraction where MAXIMUM ACCURACY is required (no simplifications)
- Highly versatile tool – ideal solution for
  - Via capacitance analysis on 45nm technologies and below (via capacitance is now a significant source of capacitive delay)
  - Low Voltage – High Speed parasitic analysis for deep sub-micron (Parasitics now dominate delays and signal noise)
  - True 3D process effects are important for accurate SPICE results
  - TFT pixel arrays where many conformal depositions make capacitance analysis using traditional rule based tools too inaccurate due to multiple topology effects