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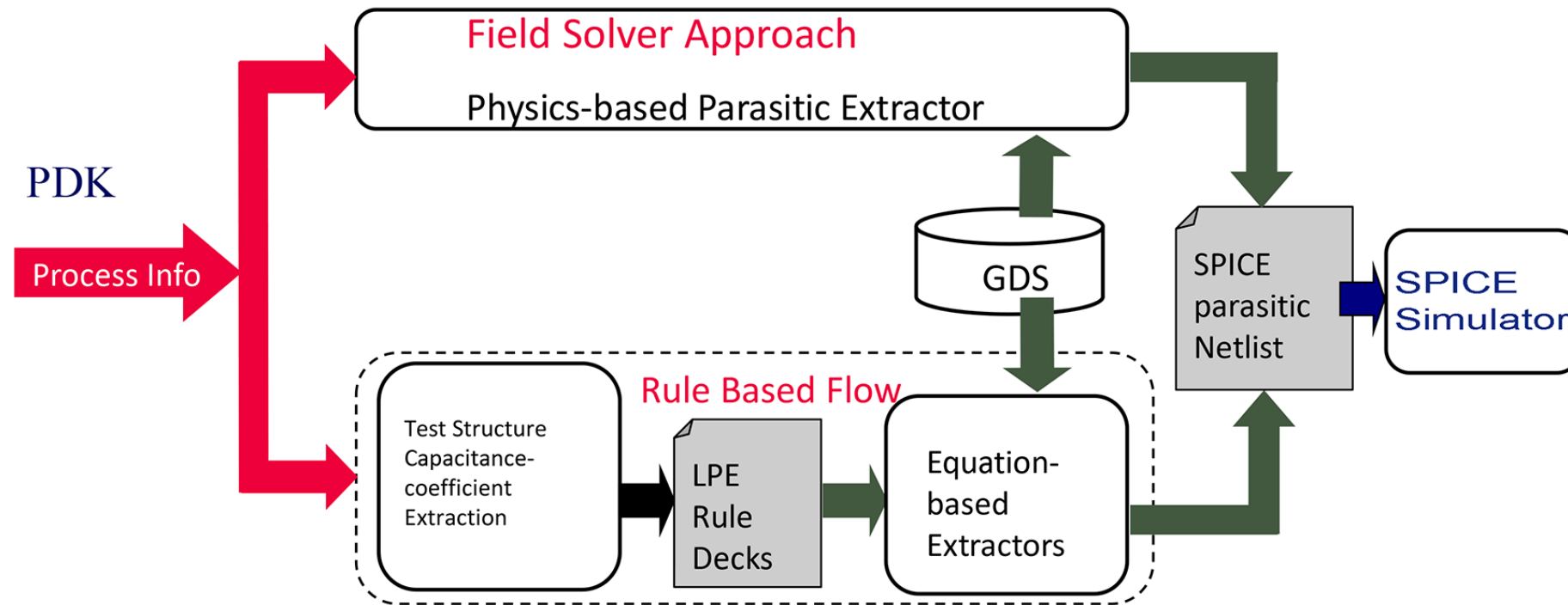
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# Introduction

- Many Solution Methodologies Exist for RCX Extraction
- No One Methodology is Suitable for all Circuit Blocks
- Combine Solution Methods for each Cell or Block
- Common Integrated Platform to Localize User Options
- Consider Intended User Skill Set, CAD versus TCAD
- Consider Size and Topology, versus Simulation Speed
- How Much Accuracy do you Really Need ?
- User Choices are Often Technology Dependent

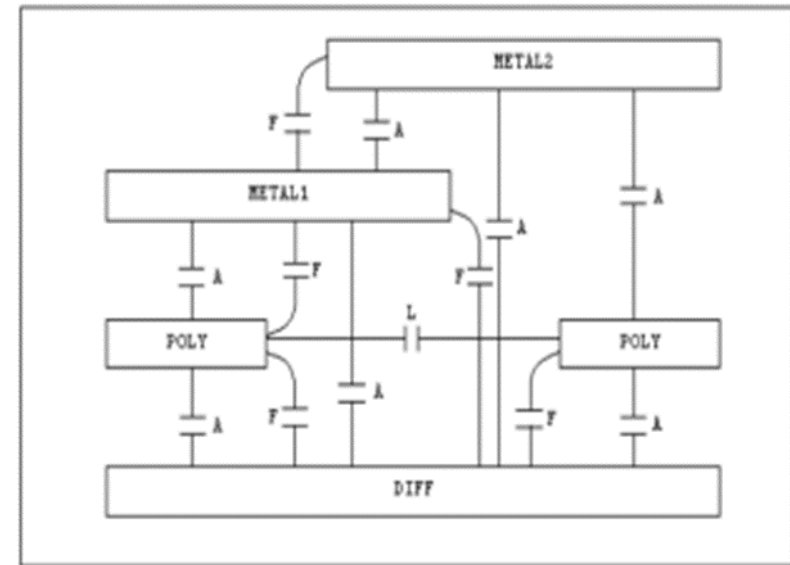
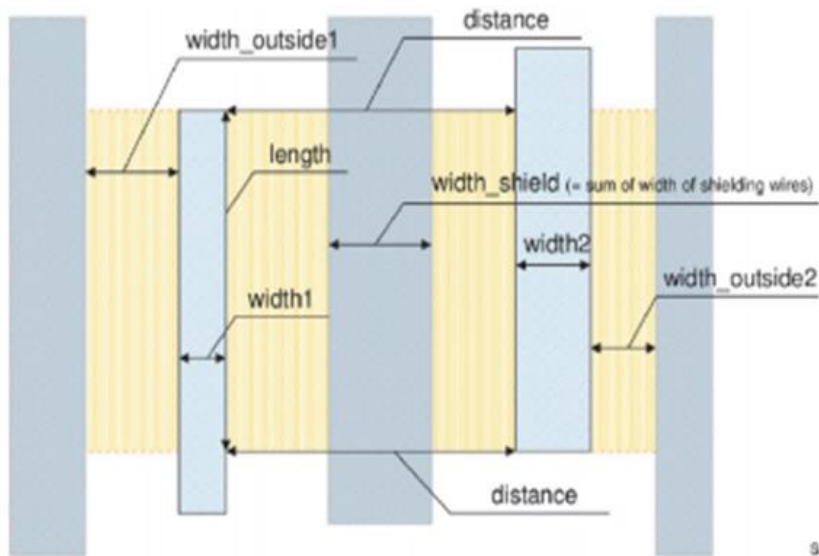
# Solution Methodologies

- Rule Based - or - Field Solver Based

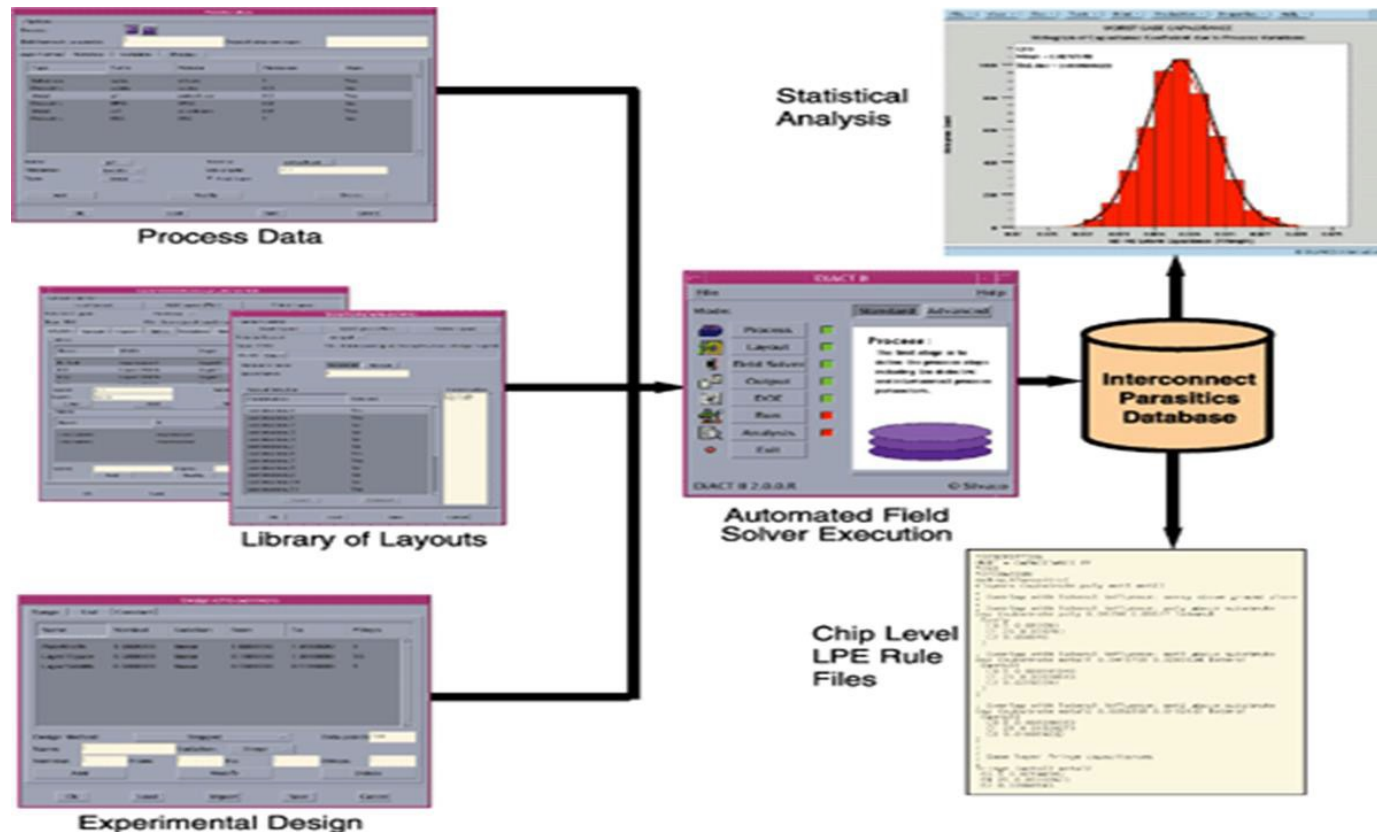


# Rule Based

- Capacitance Extract Geometry from layout Polygons
- Resistance Count Conductor Length in “Squares”
- Coefficient Database Converts Polygons into C and R



# Generating Parasitic Database



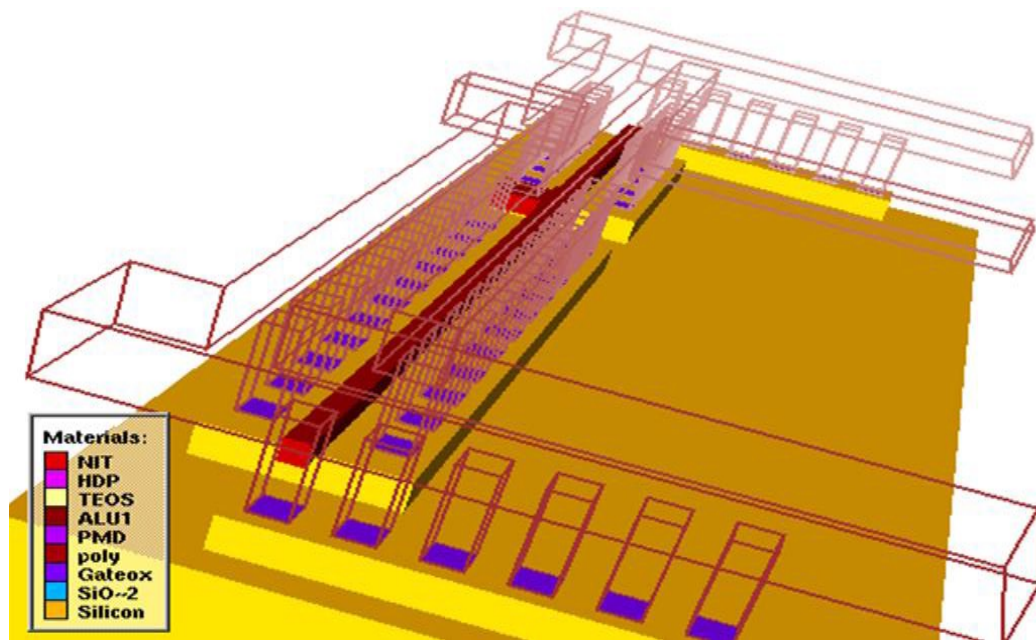
- However, generating the large capacitance coefficient database for rule based extraction, also requires a specific field solver solution, one time per technology

# Field Solver Methods

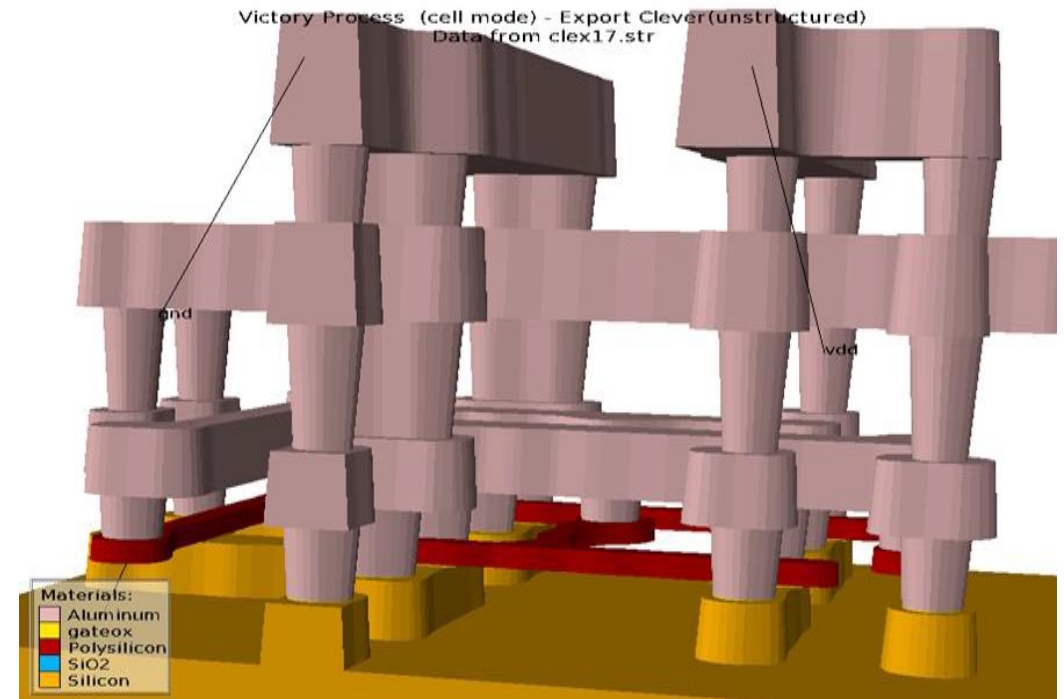
- Field Solver's have several methods to apply the physics to
- the Physical Representation of the Structure
- Field Solvers Extract Both Capacitance and Resistance
- Finite Difference and Finite Element Methods are:
  - Optimal for Complex and Curved 3D Shapes
- Boundary Element and Random Walk Methods are:
  - Optimal for Squared Off Simple “Manhattan” Shapes
- Simulation Speed versus Shape Complexity Trade off
- Silvaco uses Field Solvers from Both Category Types

# Boundary Element or Finite Element ?

- For Uniform Layer Thickness and Manhattan Shapes
  - Boundary Element Method



- For Complex 3D Shapes
  - Finite Element Method





# Combining Both Rule and Field Solver Methods

- Technology information for field solved sections can be defined in several ways:
  - 1/ Using TCAD tools and syntax (Left)
  - 2/ Using a GUI in the Layout Tool (Below)
  - 3/ A file provided from the PDK
- Choices for TCAD or CAD Engineers

```

12 # Trench Etch
13 lithography mask=AA maskcriticalintensity=0.5 maskaperture=0.5
14 \
15     maskdefocus=0 wavelength=0.248
16 Etch material=Silicon Thickness=0.5 angle=87 dry mask=AA_LITHO
17 \
18     tolerance=$accuracy
19 # Intrinsic gate oxide capacitance is already in Spice Model
20 card, so
21 # create a low permittivity active gate oxide layer to remove
22 intrinsic Cox
23 Deposit material=Oxide Thickness=0 Max
24 Deposit Material=Gateox Thickness=0.01 Max
25 Etch material=Gateox Thickness=0.1 max mask=*GATE reverse
26 Deposit material=Oxide Thickness=0 Max
27
28 # Poly Gate formation
29 Deposit material=Poly Thickness=0.2 Max
30 lithography mask=poly maskcriticalintensity=0.5 maskaperture=
31 0.5 \
32     maskdefocus=0 wavelength=0.248
33 Etch material=Polysilicon Thick=0.22 angle=87 dry mask=
34 poly_LITHO \
35     tolerance=$accuracy
36 Electrodes mask=*GATE material=Polysilicon
37
38 # Contacts
39 Deposit material=Oxide Thickness=0.4 Max
40 lithography mask=cont reverse maskcriticalintensity=0.5
41 maskaperture=0.5 \
42     maskdefocus=0 wavelength=0.248
    
```

Line: 0 Column: 1 Ready No files generated Free space : 22.6 TB DeckBuild 5.2.13.R Copyright © 1984 - 2021 silvaco

Process Simulation Setup - [default] (pbe01.Silvaco.COM)

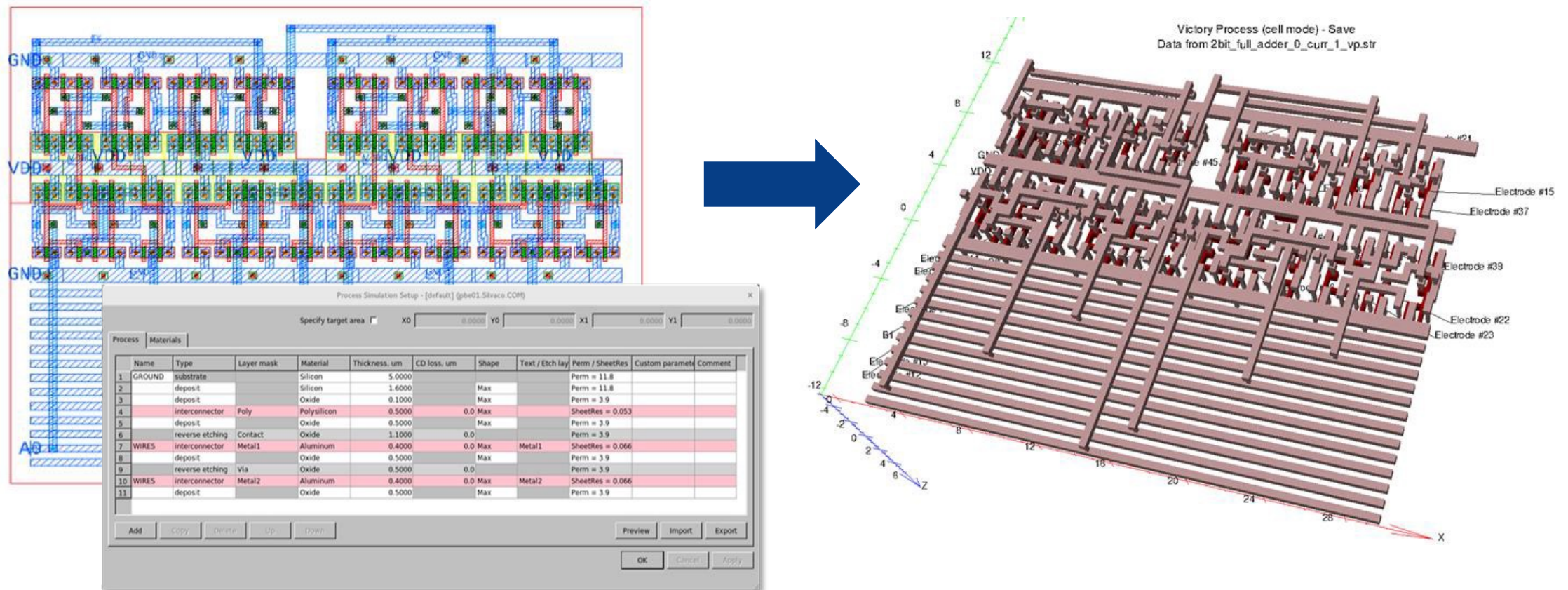
Specify target area  X0: 0.0000 Y0: 0.0000 X1: 0.0000 Y1: 0.0000

Name	Type	Layer mask	Material	Thickness, um	CD loss, um	Shape	Text / Etch lay	Perm / SheetRes	Custom paramet	Comment
1	GROUND	substrate	Silicon	5.0000				Perm = 11.8		
2		deposit	Silicon	1.6000		Max		Perm = 11.8		
3			Oxide	0.1000		Max		Perm = 3.9		
4		interconnector	Poly	Polysilicon	0.5000	0.0 Max		SheetRes = 0.053		
5		deposit	Oxide	0.5000		Max		Perm = 3.9		
6		reverse etching	Contact	Oxide	1.1000	0.0		Perm = 3.9		
7	WIRES	interconnector	Metal1	Aluminum	0.4000	0.0 Max	Metal1	SheetRes = 0.066		
8		deposit	Oxide	0.5000		Max		Perm = 3.9		
9		reverse etching	Via	Oxide	0.5000	0.0		Perm = 3.9		
10	WIRES	interconnector	Metal2	Aluminum	0.4000	0.0 Max	Metal2	SheetRes = 0.066		
11		deposit	Oxide	0.5000		Max		Perm = 3.9		

Buttons: Add, Copy, Delete, Up, Down, Preview, Import, Export, OK, Cancel, Apply

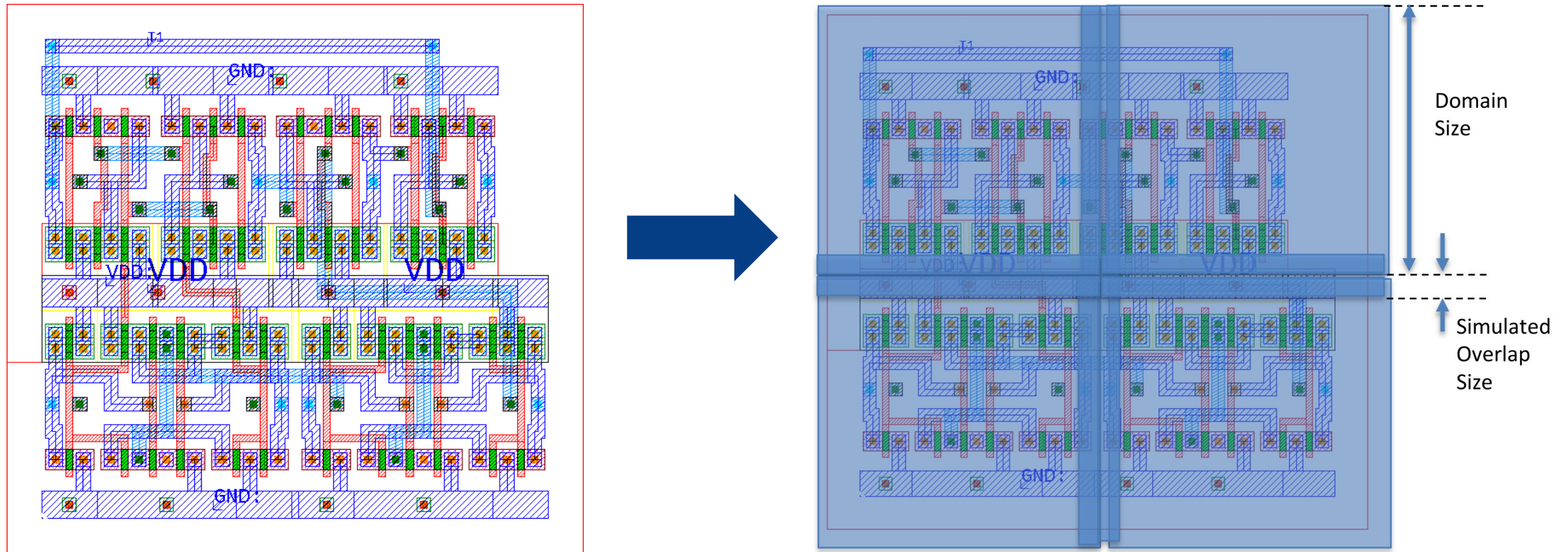
# Combining Both Rule and Field Solver Methods

- Technology information plus layout is converted into a true 3D model of the BEOL for Field Solve



# Combining Both Rule and Field Solver Methods

- Domain decomposition allows much larger circuit sections to be field solved





# Combining Both Rule and Field Solver Methods

- True Mix and Match Capability in One Tool

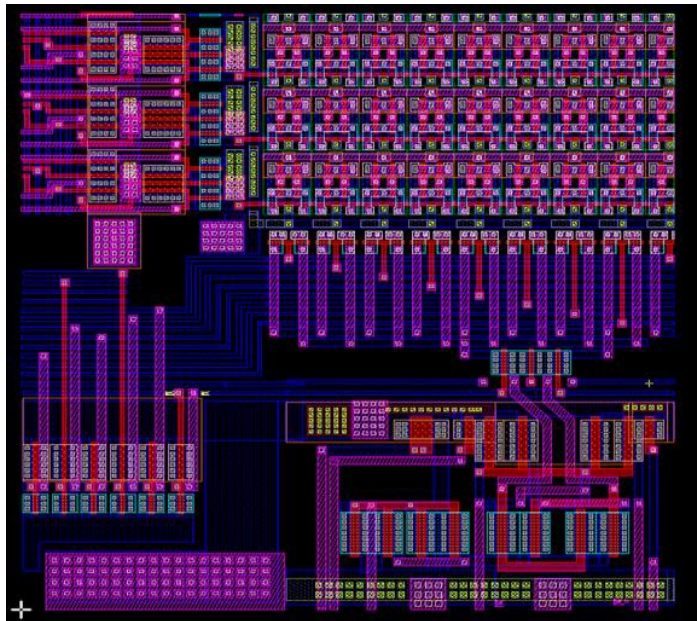
User selects which section of the layout is solved using finite element or boundary element field solvers, with the remainder using traditional rule based extraction

The screenshot shows the 'Parasitic Extraction (Capacitance)' dialog box. The 'Field Solver' section is active, with 'Stellar' selected. The 'Decomposition' section is highlighted with a red box, showing 'Stripes' and 'Boxes' options. The 'Mix-and-Match' section is also active, showing a table of solver configurations. Three yellow arrows point from the 'Stellar' and 'Clever' rows in the table to the corresponding regions in the layout diagram on the right, which is labeled 'Stellar', 'Victory RCx Pro', and 'Rule-based'.

MinX	MinY	MaxX	MaxY	OverlapX	OverlapY	Extraction	Options	SizeX	SizeY	VcinityX	VcinityY
100.000	420.000	566.000	566.000	40.000	20.000	Stellar	...	233.000	146.000	30.000	20.000
52.000	196.000	530.000	360.000	45.000	30.000	Clever	...	240.000	82.000	40.000	25.000

# Summary

- Rule Based Extraction Use for Most of the Full Chip
- Field Solver Extraction Complex R and C Topology
  - Where Highest Accuracy is Required for Critical Cells
- Mix and Match Techniques within One Design



Typical Maximum Cell Size illustration for using Field Solve Techniques

