SILVACO

Parasitic Extraction Victory RCx Pro and Hipex FS

Integrated Full Chip and Cell Level RCX
Combine Rule Based and Field Solver Solutions

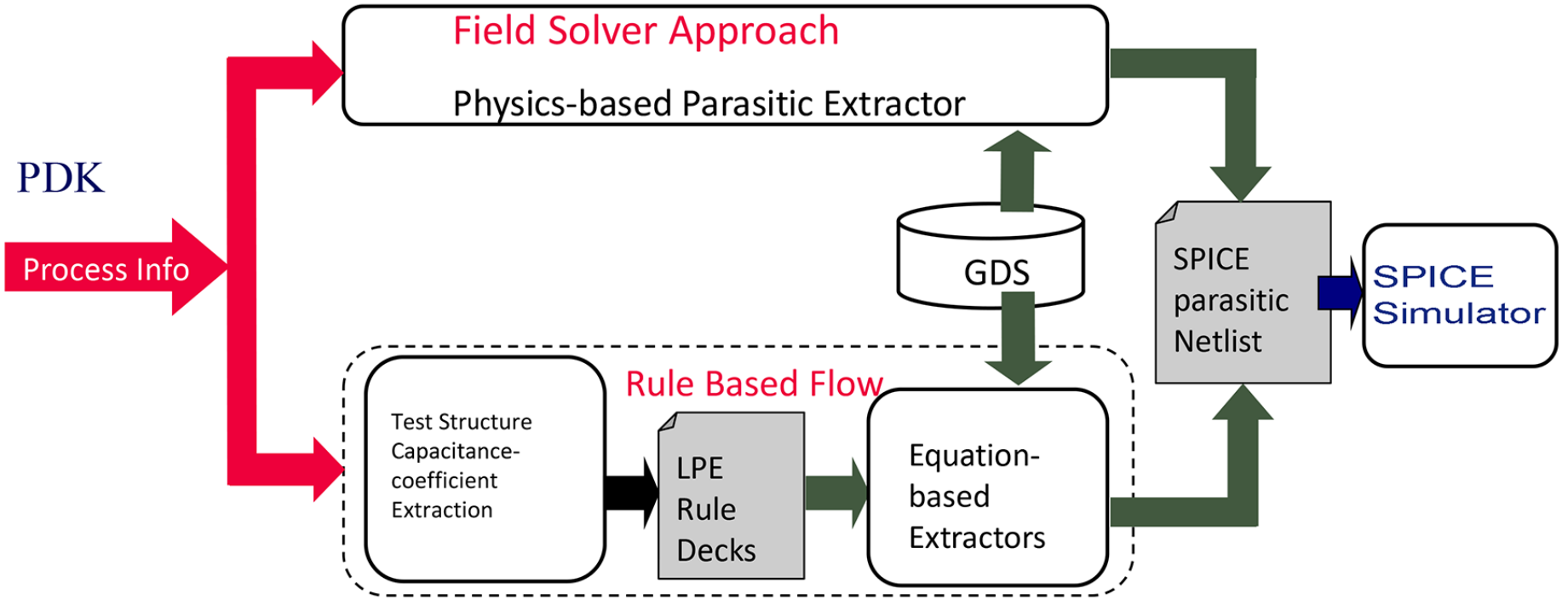
Contents

Introduction

- Many Solution Methodologies Exist for RCX Extraction
- No One Methodology is Suitable for all Circuit Blocks
- Combine Solution Methods for each Cell or Block
- Common Integrated Platform to Localize User Options
- Consider Intended User Skill Set, CAD versus TCAD
- Consider Size and Topology, versus Simulation Speed
- How Much Accuracy do you Really Need ?
- User Choices are Often Technology Dependent

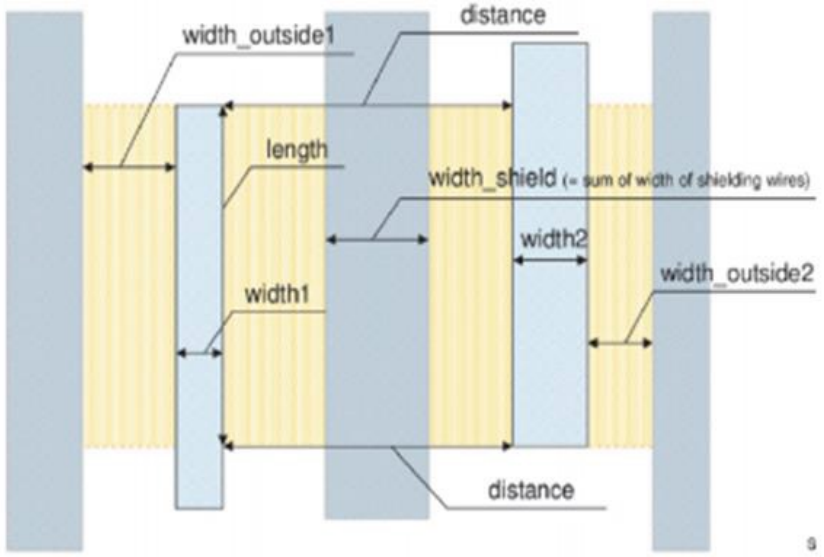
Solution Methodologies

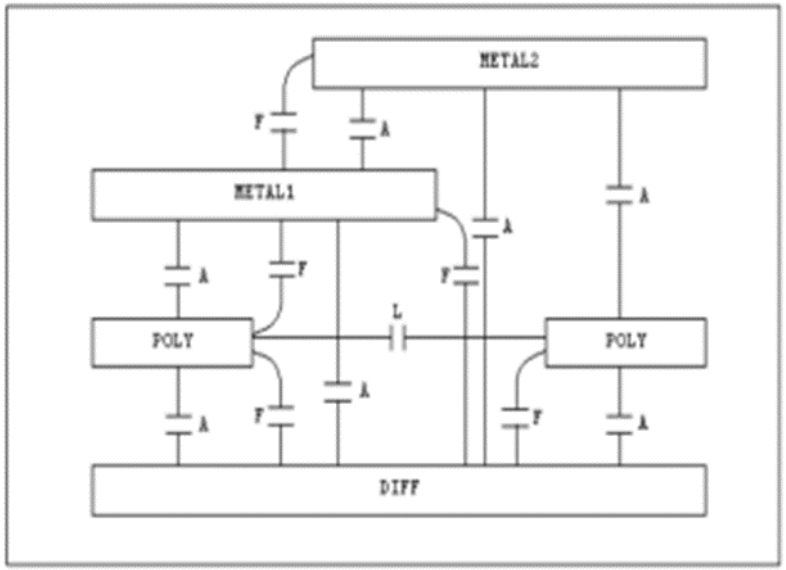
- Rule Based - or - Field Solver Based



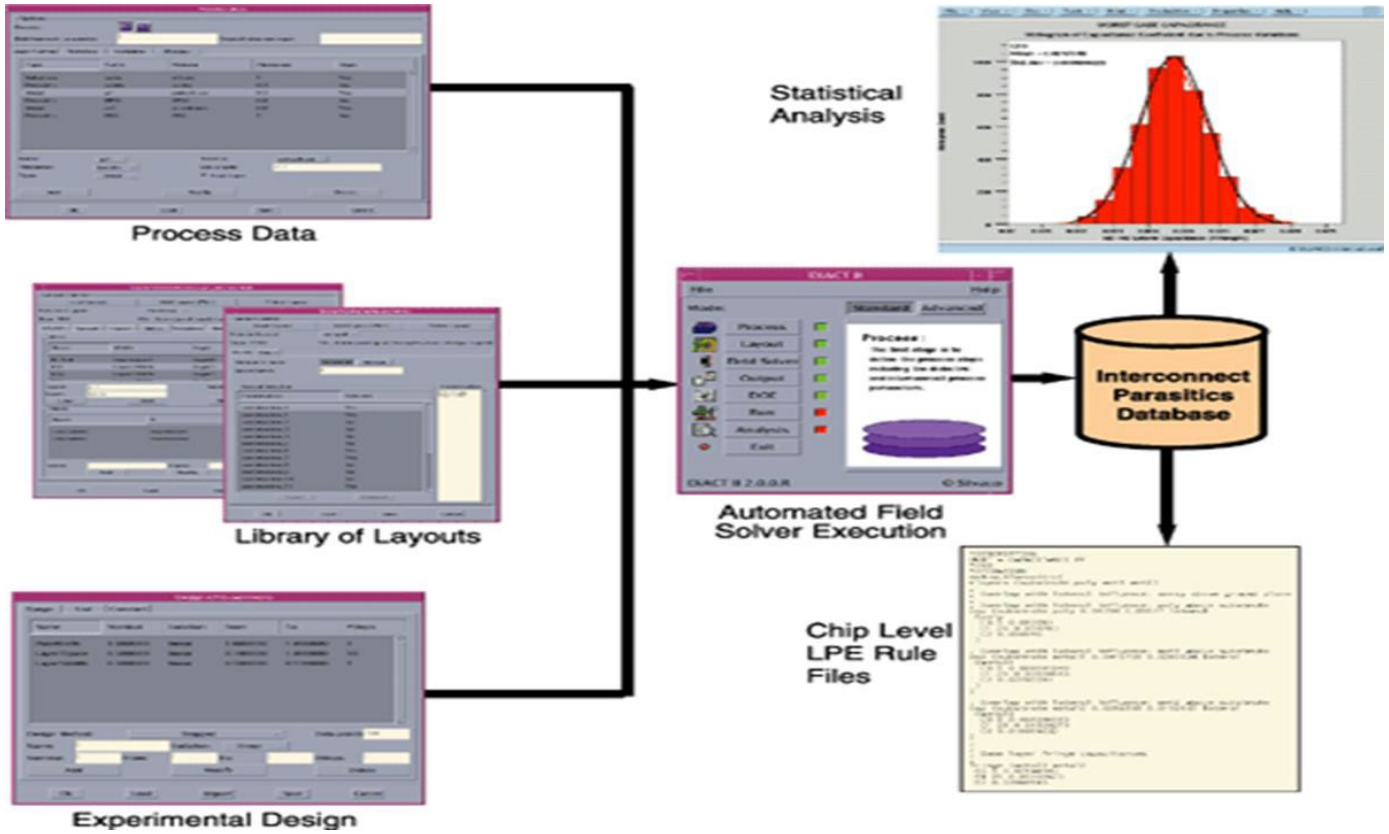
Rule Based

- Capacitance Extract Geometry from layout Polygons
- Resistance Count Conductor Length in “Squares”
- Coefficient Database Converts Polygons into C and R





Generating Parasitic Database



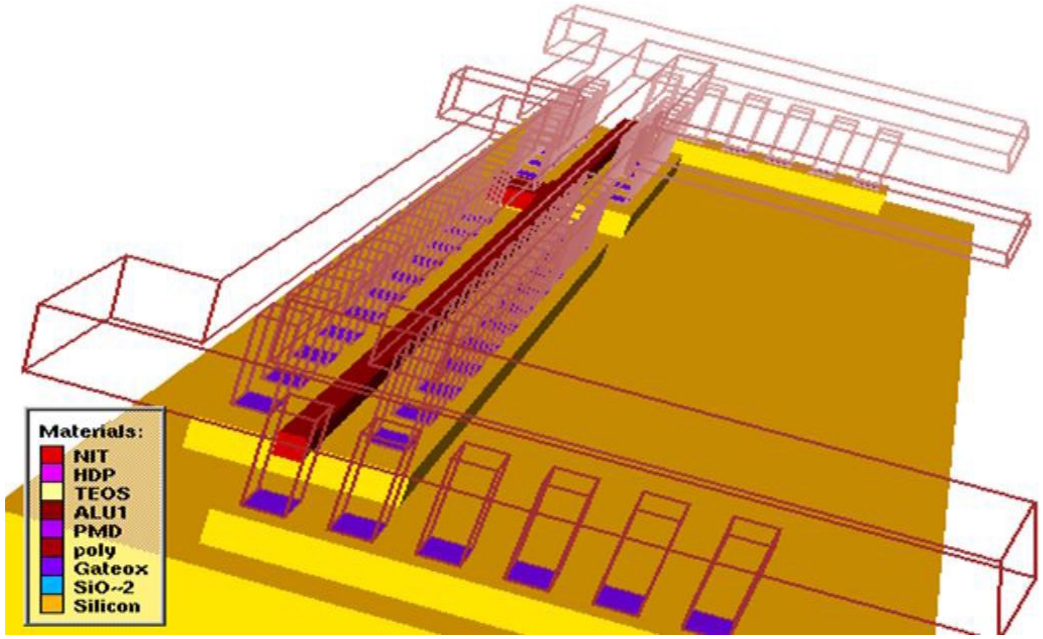
- However, generating the large capacitance coefficient database for rule based extraction, also requires a specific field solver solution, one time per technology

Field Solver Methods

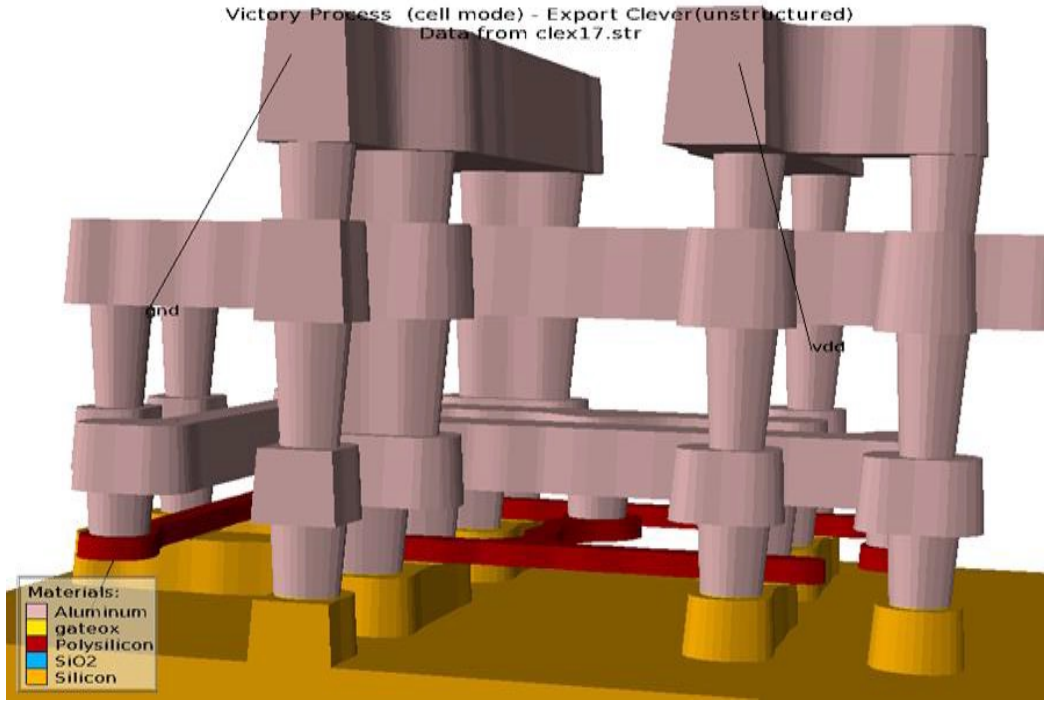
- Field Solver's have several methods to apply the physics to
- the Physical Representation of the Structure
- Field Solvers Extract Both Capacitance and Resistance
- Finite Difference and Finite Element Methods are:
  - Optimal for Complex and Curved 3D Shapes
- Boundary Element and Random Walk Methods are:
  - Optimal for Squared Off Simple "Manhattan" Shapes
- Simulation Speed versus Shape Complexity Trade off
- Silvaco uses Field Solvers from Both Category Types

Boundary Element or Finite Element ?

- For Uniform Layer Thickness and Manhattan Shapes
  - Boundary Element Method



- For Complex 3D Shapes
  - Finite Element Method



Combining Both Rule and Field Solver Methods

File Edit View Run Tools Commands Help

Connect

Deck

```
12  # Trench Etch
13  lithography mask=AA maskcriticalintensity=0.5 maskaperture=0.5
     \
14                maskdefocus=0 wavelength=0.248
15  Etch material=Silicon Thickness=0.5 angle=87 dry mask=AA_LITHO
     \
16      tolerance=$accuracy
17
18  # Intrinsic gate oxide capacitance is already in Spice Model
    card, so
19  # create a low permittivity active gate oxide layer to remove
    intrinsic Cox
20  Deposit material=Oxide Thickness=0 Max
21  Deposit Material=Gateox Thickness=0.01 Max
22  Etch material=Gateox Thickness=0.1 max mask=*GATE reverse
23  Deposit material=Oxide Thickness=0 Max
24
25  # Poly Gate formation
26  Deposit material=Poly Thickness=0.2 Max
27  lithography mask=poly maskcriticalintensity=0.5 maskaperture=
    0.5 \
28                maskdefocus=0 wavelength=0.248
29  Etch material=Polysilicon Thick=0.22 angle=87 dry mask=
    poly_LITHO \
30      tolerance=$accuracy
31  Electrodes mask=*GATE material=Polysilicon
32
33  # Contacts
34  Deposit material=Oxide Thickness=0.4 Max
35  lithography mask=cont reverse maskcriticalintensity=0.5
    maskaperture=0.5 \
36                maskdefocus=0 wavelength=0.248
```

Variables history

Outputs

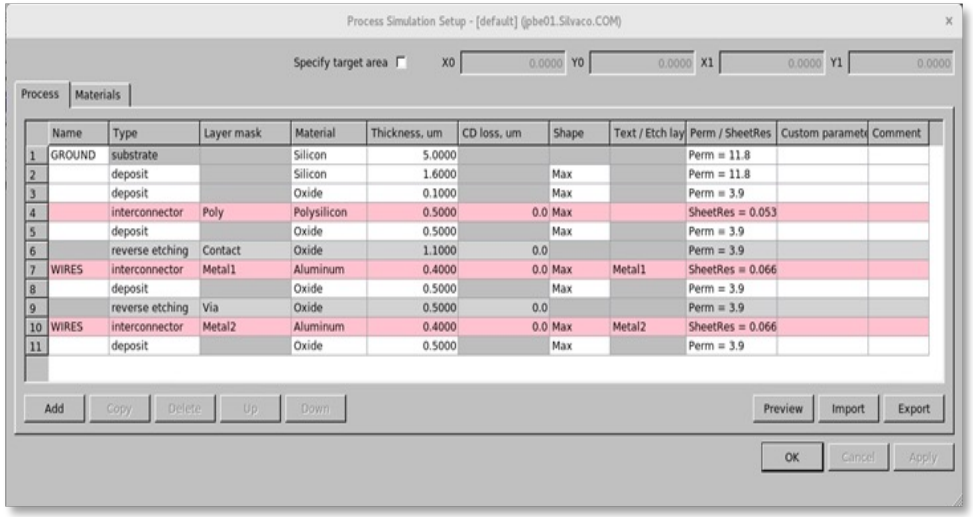
Filter: *.str, *.log Default Filter

Resource usage

0 bytes Memory | 0 bytes/s IO read | 0 bytes/s IO write

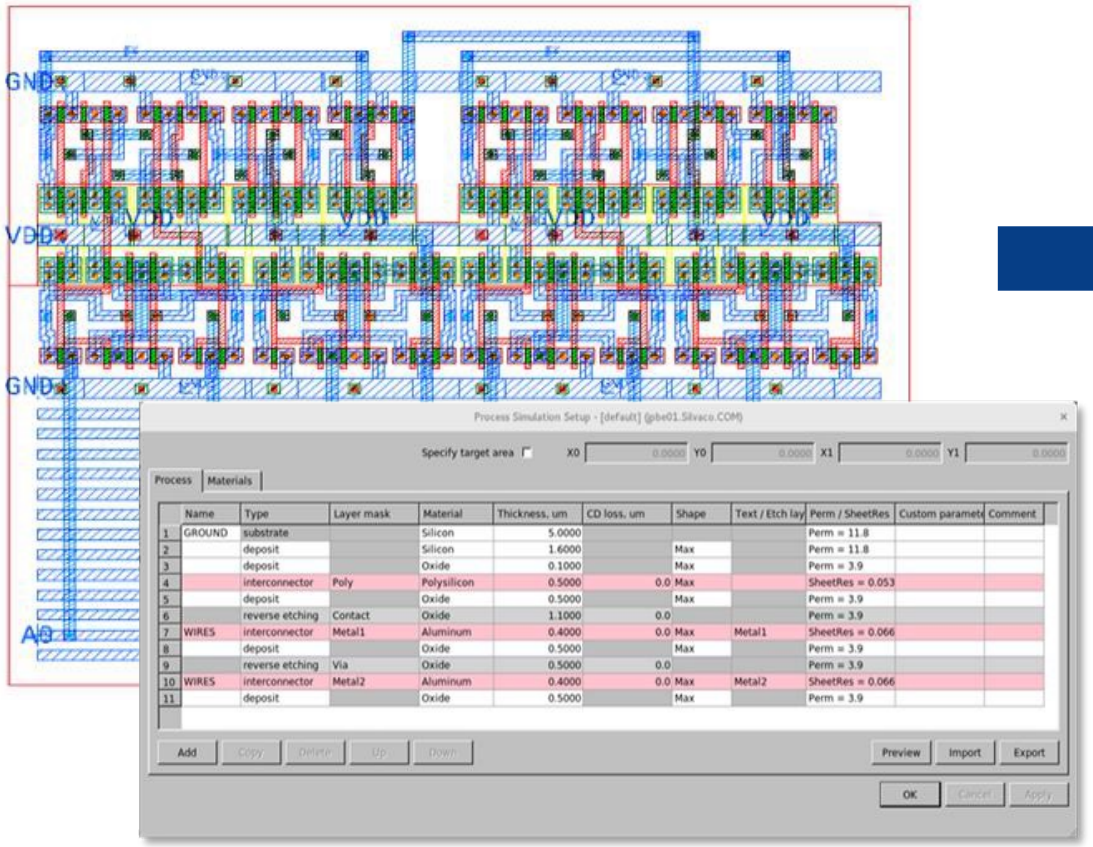
Line: 0 Column: 1 Ready No files generated Free space : 22.6 TB DeckBuild 5.2.13.R Copyright © 1984 - 2021 silvaco

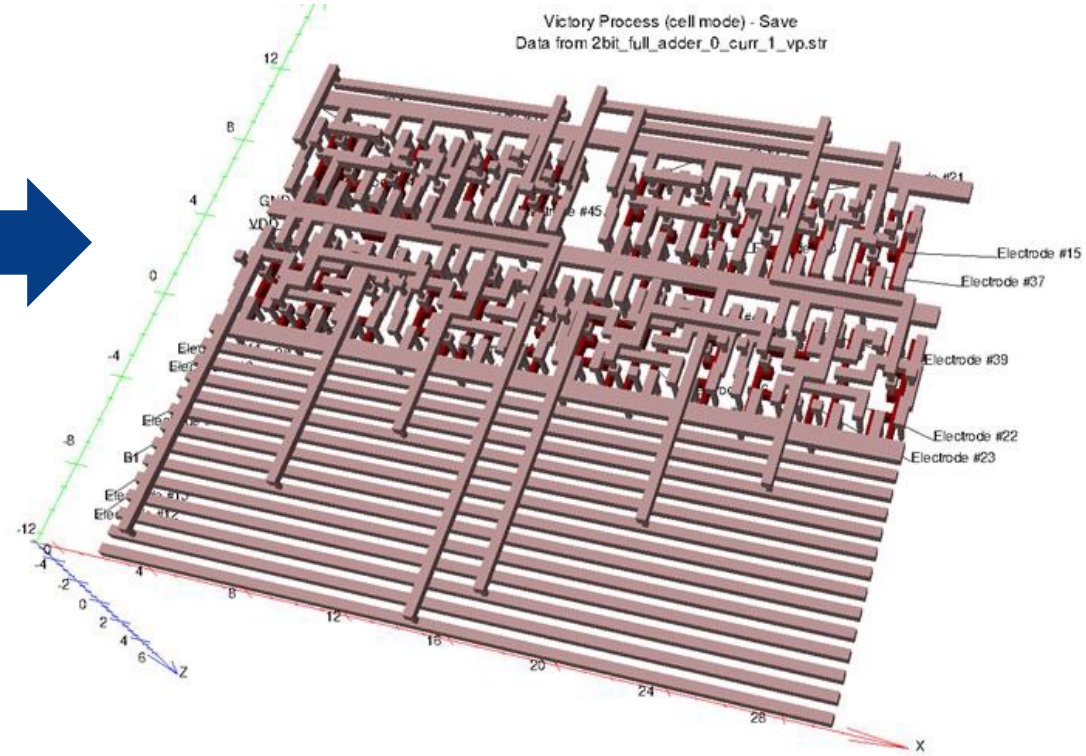
- Technology information for field solved sections can be defined in several ways:
  - 1/ Using TCAD tools and syntax (Left)
  - 2/ Using a GUI in the Layout Tool (Below)
  - 3/ A file provided from the PDK
- Choices for TCAD or CAD Engineers



Combining Both Rule and Field Solver Methods

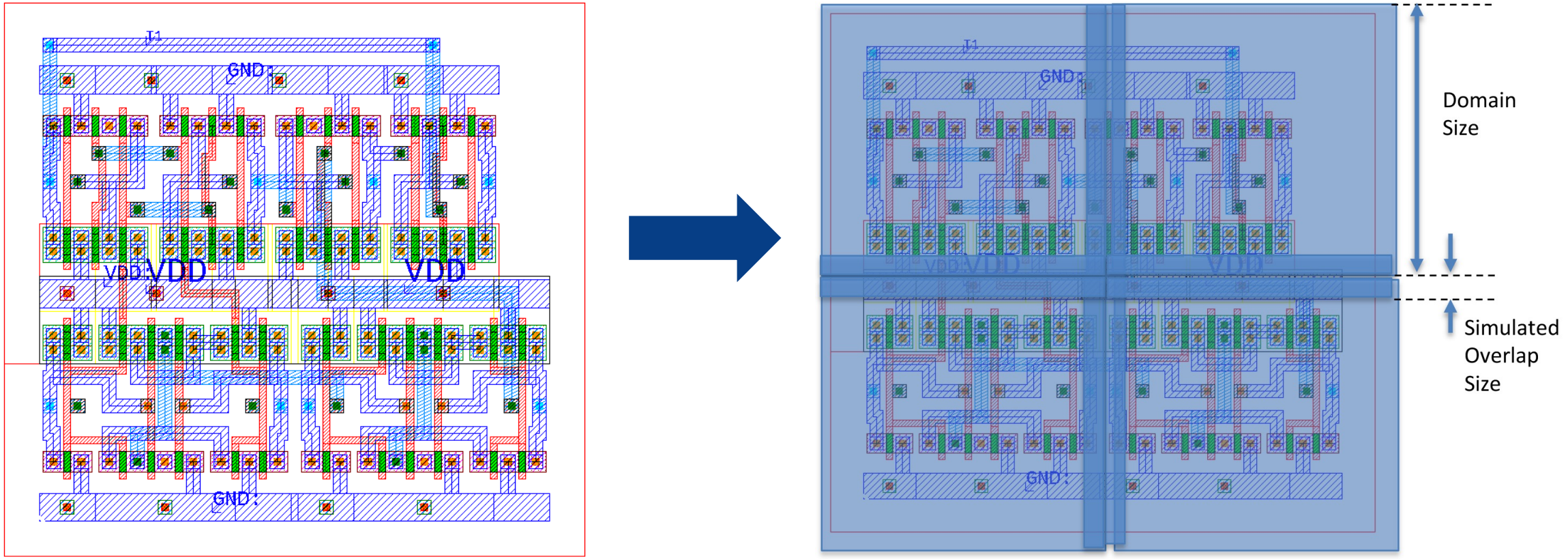
- Technology information plus layout is converted into a true 3D model of the BEOL for Field Solve





Combining Both Rule and Field Solver Methods

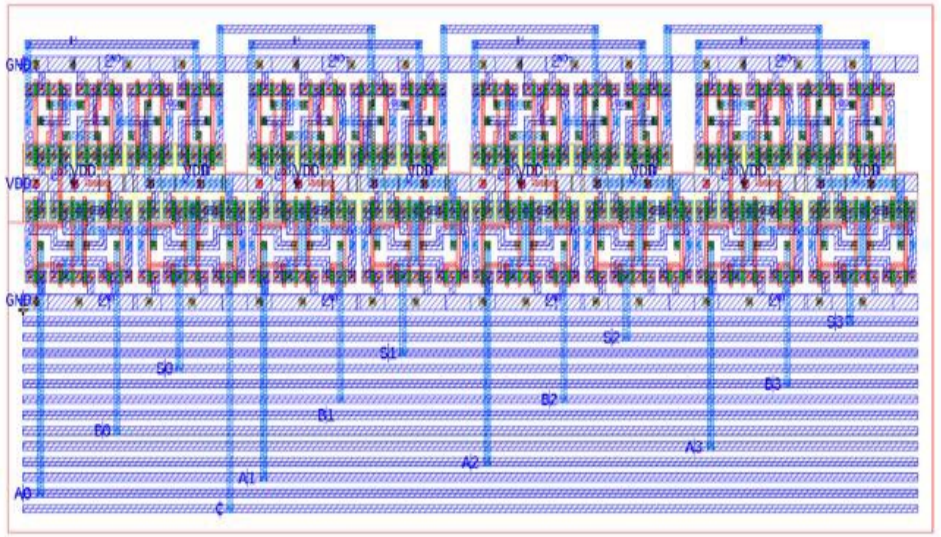
- Domain decomposition allows much larger circuit sections to be field solved

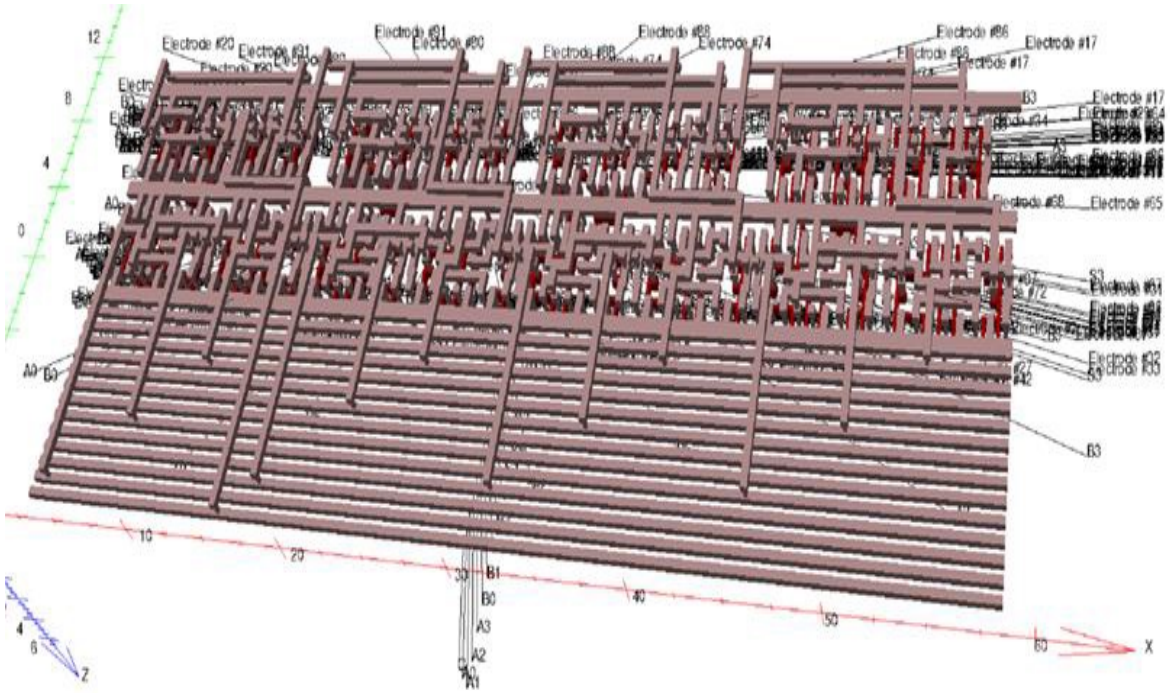


Combining Both Rule and Field Solver Methods

- Simulating a larger overlap improves accuracy a little at the expense of simulation speed.

Example of full 4 bit adder below, using boundary element method, simulation time 26 minutes, 41 seconds using 4 CPUs

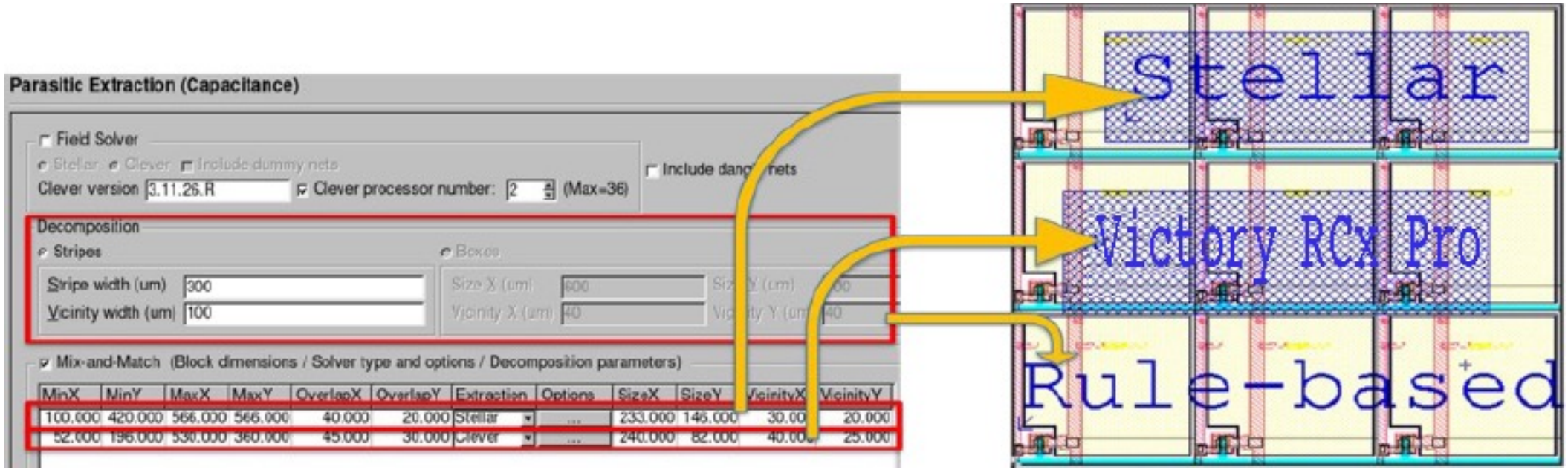




Combining Both Rule and Field Solver Methods

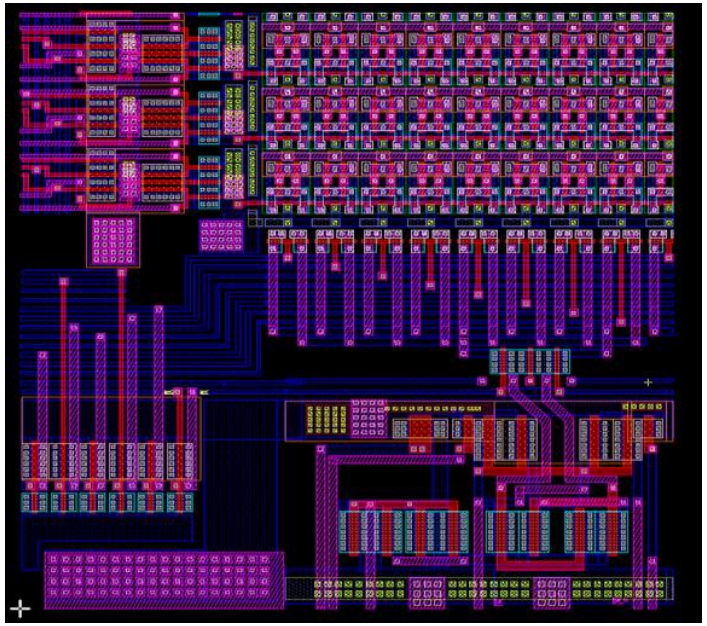
- True Mix and Match Capability in One Tool

User selects which section of the layout is solved using finite element or boundary element field solvers, with the remainder using traditional rule based extraction



Summary

- Rule Based Extraction Use for Most of the Full Chip
- Field Solver Extraction Complex R and C Topology
  - Where Highest Accuracy is Required for Critical Cells
- Mix and Match Techniques within One Design



Typical Maximum Cell Size illustration for using Field Solve Techniques