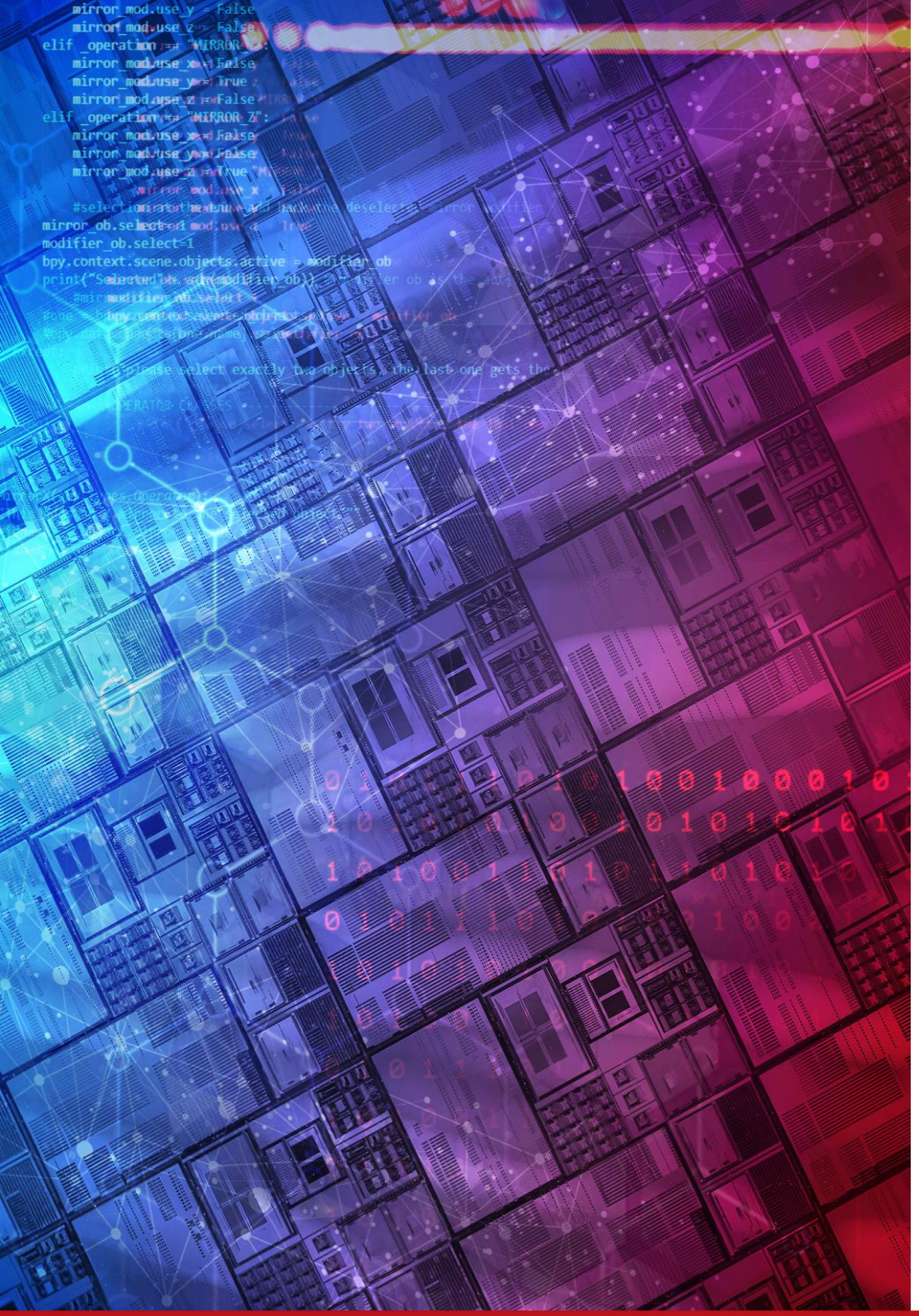

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SmartDRC and SmartLVS

Physical Verification Tools

Contents

- SmartDRC/LVS technology overview
- SmartDRC/LVS capabilities
- Performance / capacity
- Rule coverage
- Foundry Support
- Summary

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SmartDRC/LVS
Technology Overview

- Silvaco acquired PolytEDA in Q1 2021. The entire Kiev R&D team has joined SILVACO as the result of acquisition.

- Now introducing SmartDRC/LVS and SmartRDE (Run and Debug Environment) generally available since late spring of 2021

- This is the rebranded and improved toolset formerly known as PolytEDA`s PowerDRC/LVS (on the market since 2009)

- PolytEDA came with 10 foundry-certified (sign-off) rule kits and more than 100 successful tape-outs to the date of acquisition.

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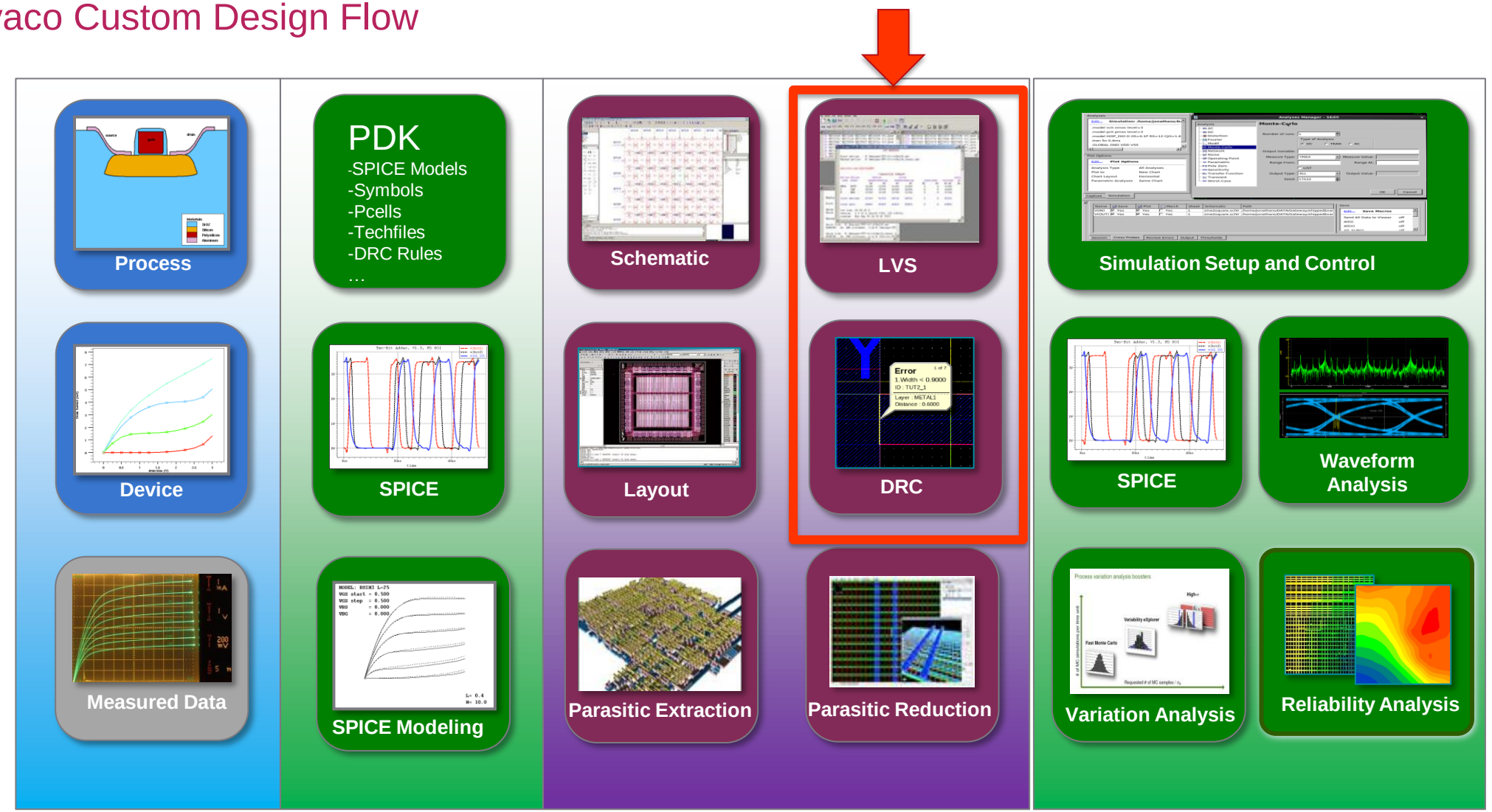
SmartDRC/LVS

Silvaco Custom Design Flow



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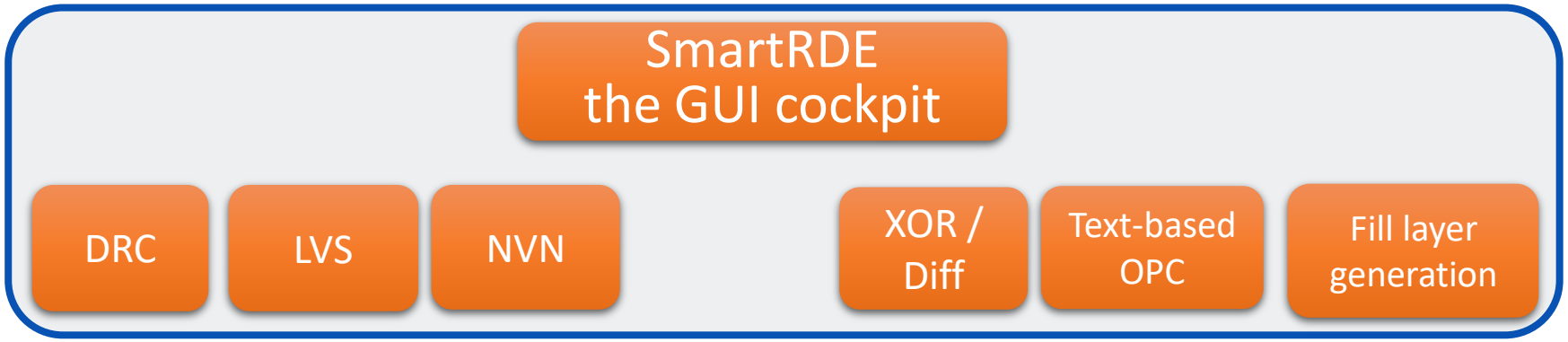
SmartDRC/LVS
Structure



- SmartDRC/LVS has a few executable files:
  - smartdrc performing DRC, ERC, LVS extraction, fillers, and LVL (XOR and Quick Diff)
  - smartnvn running LVS comparison
  - smartrde – GUI cockpit
  - couple of utilities, integration scripts

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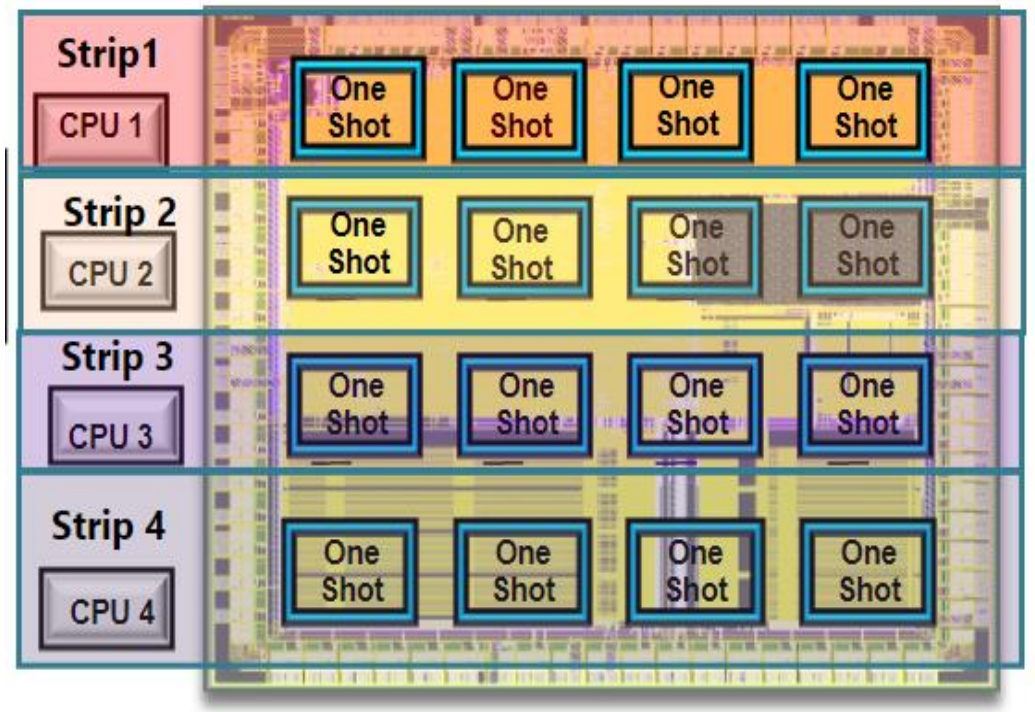
SmartDRC/LVS

Under the Hood

- Innovative layout scanning technology ensuring near-linear scaling and runtime predictability
- Combines multiple rules/layers checks
- Small and efficient memory footprint
- Processing by strips for multi-CPU
- Hierarchical processing of cell arrays and macro cells
- Processing speed is ~8-9 million transistors per hour per 1 CPU core



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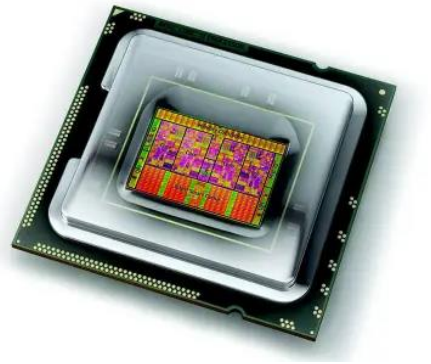
SmartDRC/LVS
Parallel Processing



SmartDRC benefits from parallel processing of:

- Independent groups of rules (blocks)
- Independent parts of layout (strips)

Parallel tasks may be run in multi-CPU mode on:

- A single multi-core host
- Multi-host multi-core platforms

- Scalability proven with up to 128 CPU cores

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SmartDRC/LVS
Batch Mode Run

- SmartDRC input
  - A set of run parameters, so called RCF - run configuration file
  - The rule file in PWRL - SmartDRC/LVS rule language
  - Layout file (GDSII, OASIS or OpenAccess)

- Command line format
  - smartdrc drc.rcf <optional commands>
  - SmartDRC output
  - Detailed log file and brief summary
  - Output file with found violations
  - Density report (if any)

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SmartDRC/LVS
Run Configuration File (RCF)

- Specifies the layout, cell to verify, rule file to use, output file
- Allows setting dozens of specific run options and variables
- Is the only required command line argument in batch mode

A simple RCF may look as follows:

```
TopCell: "sample_top";          // The cell being run
Layout:  "sample.gds";          // Input GDS file
OutputFile: "output.gds";       // Output GDS file
RuleFile: "sample_drc.pwr";     // Rule file with DRC rules
ShowAllErrorsFound: "yes";      // Write all errors found
```


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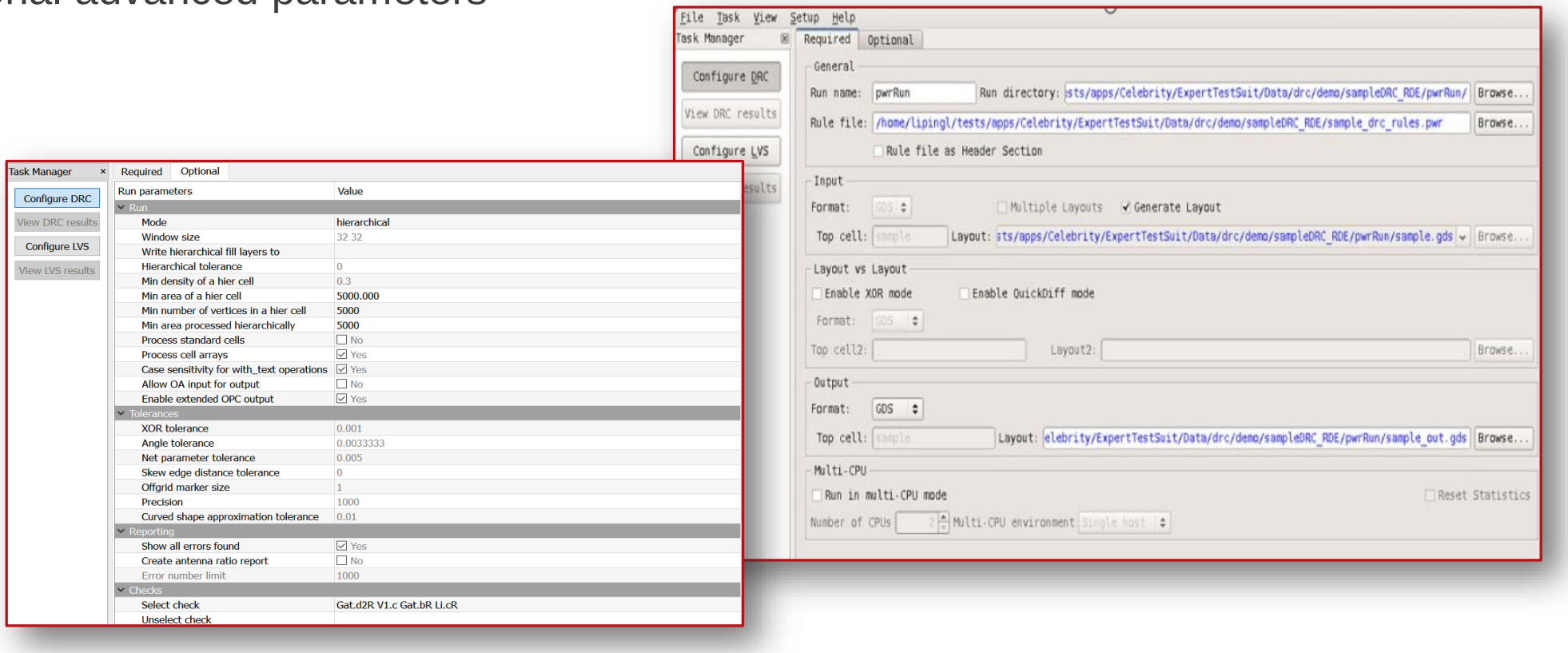
SmartRDE
Configure Your DRC Run

- Manage run settings with on-the-fly validity checks
- Set optional advanced parameters



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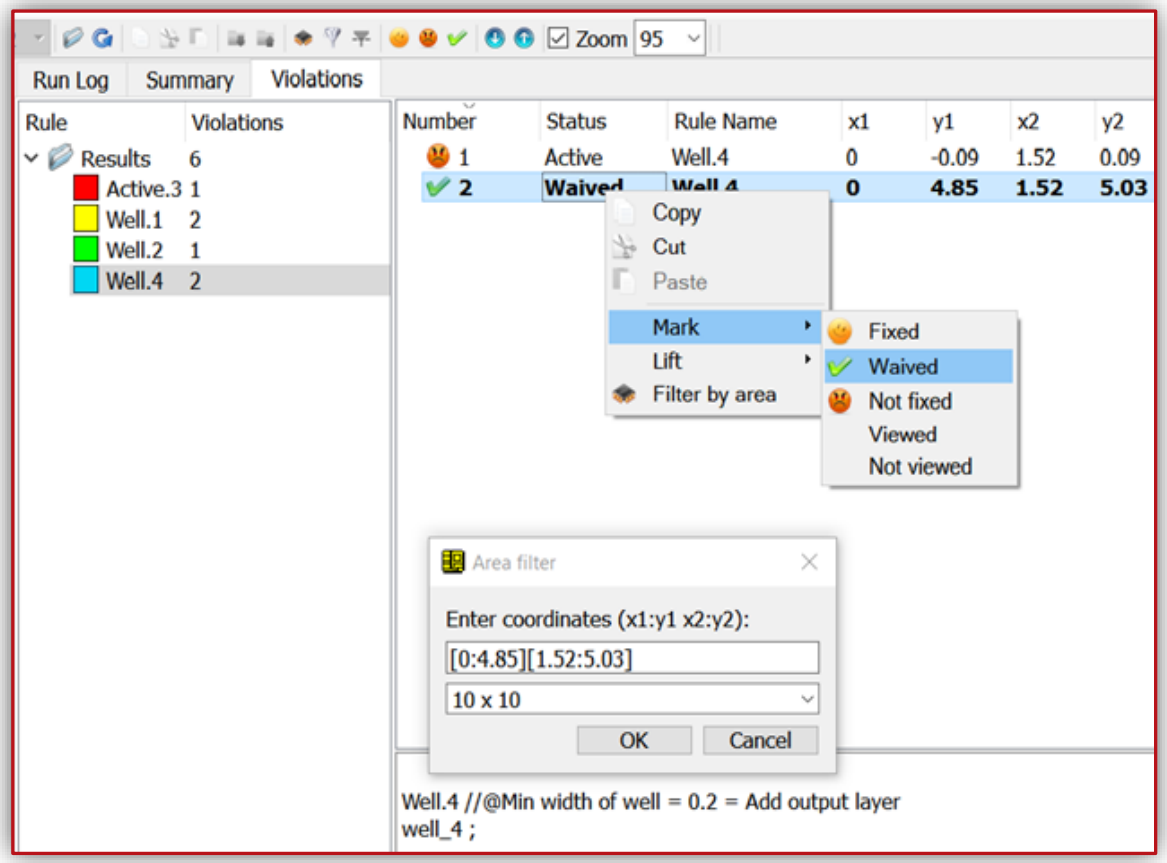
SmartRDE
View DRC Results

- Use Hierarchical error navigation
  –
- Sort, group and filter DRC violations
- Interactively debug with layout editor of choice
- Check logs and other reports



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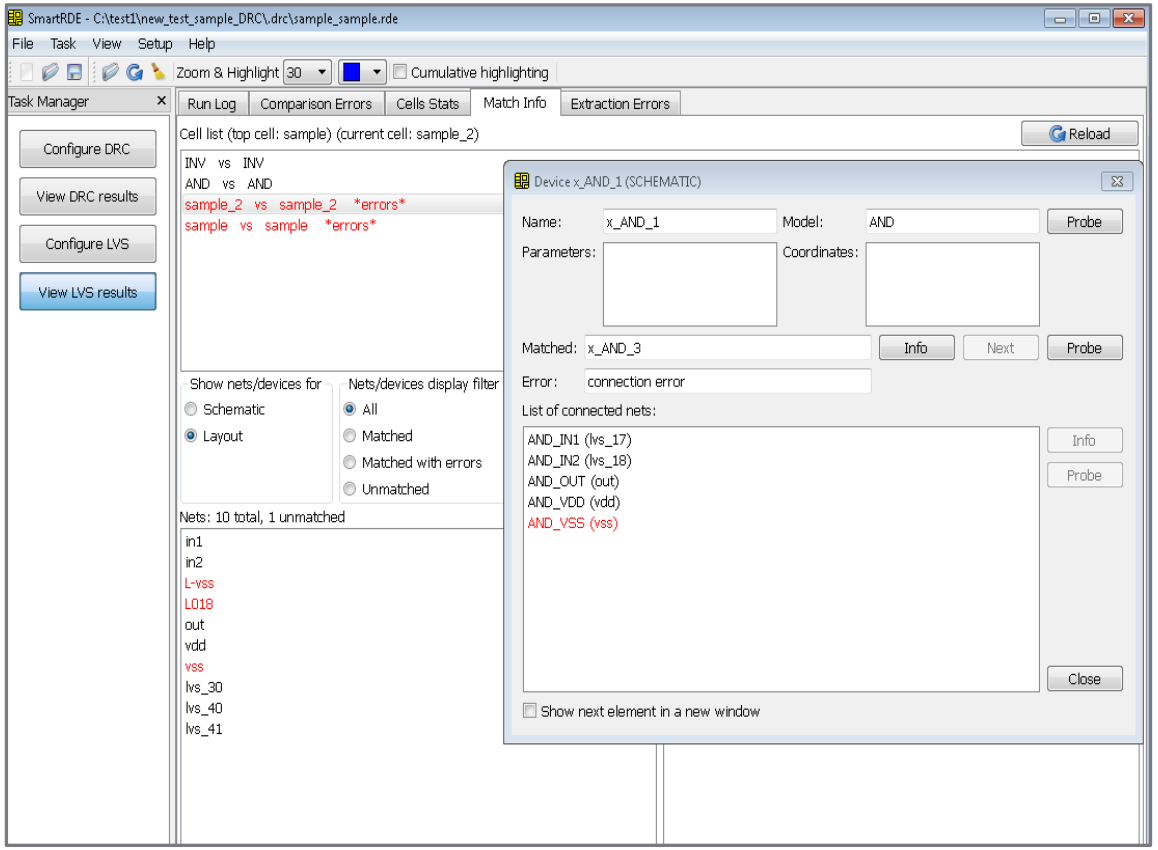
SmartRDE
Run and View LVS Results

- Manage run settings with on-the-fly validity checks
- Start LVS or NVN jobs and monitor their progress
- Extraction Errors reports with highlighting
- View and debug your LVS results from Match Info tab
- Check logs and cells statistics



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SmartDRC
Flows

- Standalone:
  - Competitive solution against higher cost options
    - 2nd source, pre-signoff
- 3rd Party Flows:
  - Integrated solution for other vendor flows
- Alternative Signoff:
  - Specific certified foundry/nodes
- Silvaco Flows:
  - Direct replacement in ACD and TCAD Flows to Guardian technology

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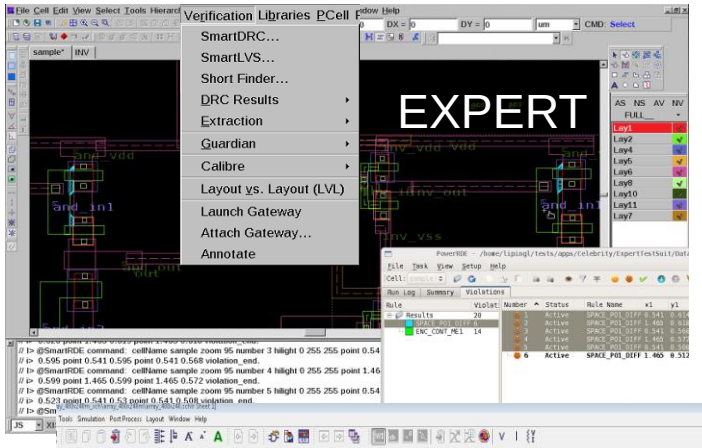
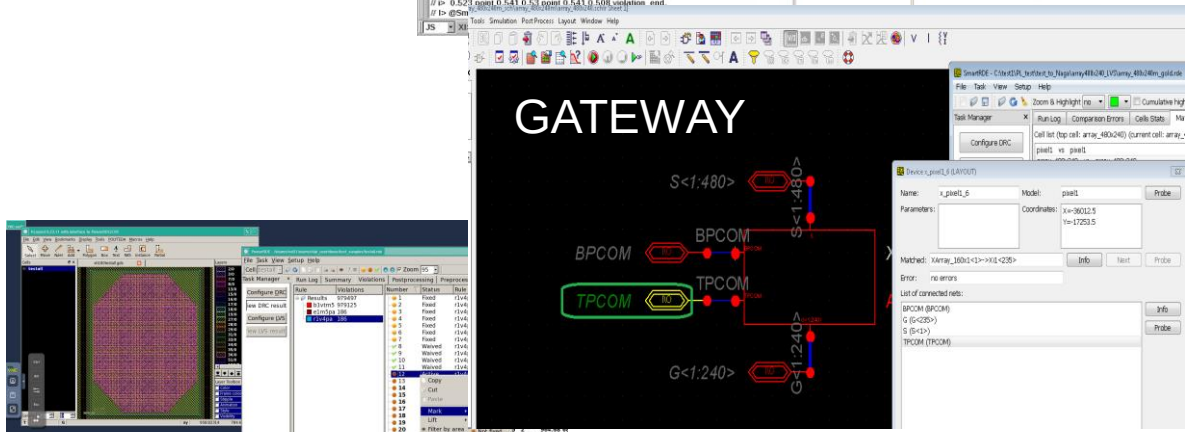
SmartDRC
Integrations

- Shipped Integrations :
  - Silvaco Gateway and Expert Editors – Native/OA
  - KLayout Editor – Native
  - Juspertor LayoutEditor – Native/OA
  - Symica DE – Native/OA
- On request
  - TexEDA LayTools – Native
  - Cadence Virtuoso – CDBA/OA
  - NI-AWR Analog Office – Native
  - Synopsys Laker – Native



DRC/LVS
- Launch
- Run
- Highlight



LVS
- Cross-probe
- Highlight

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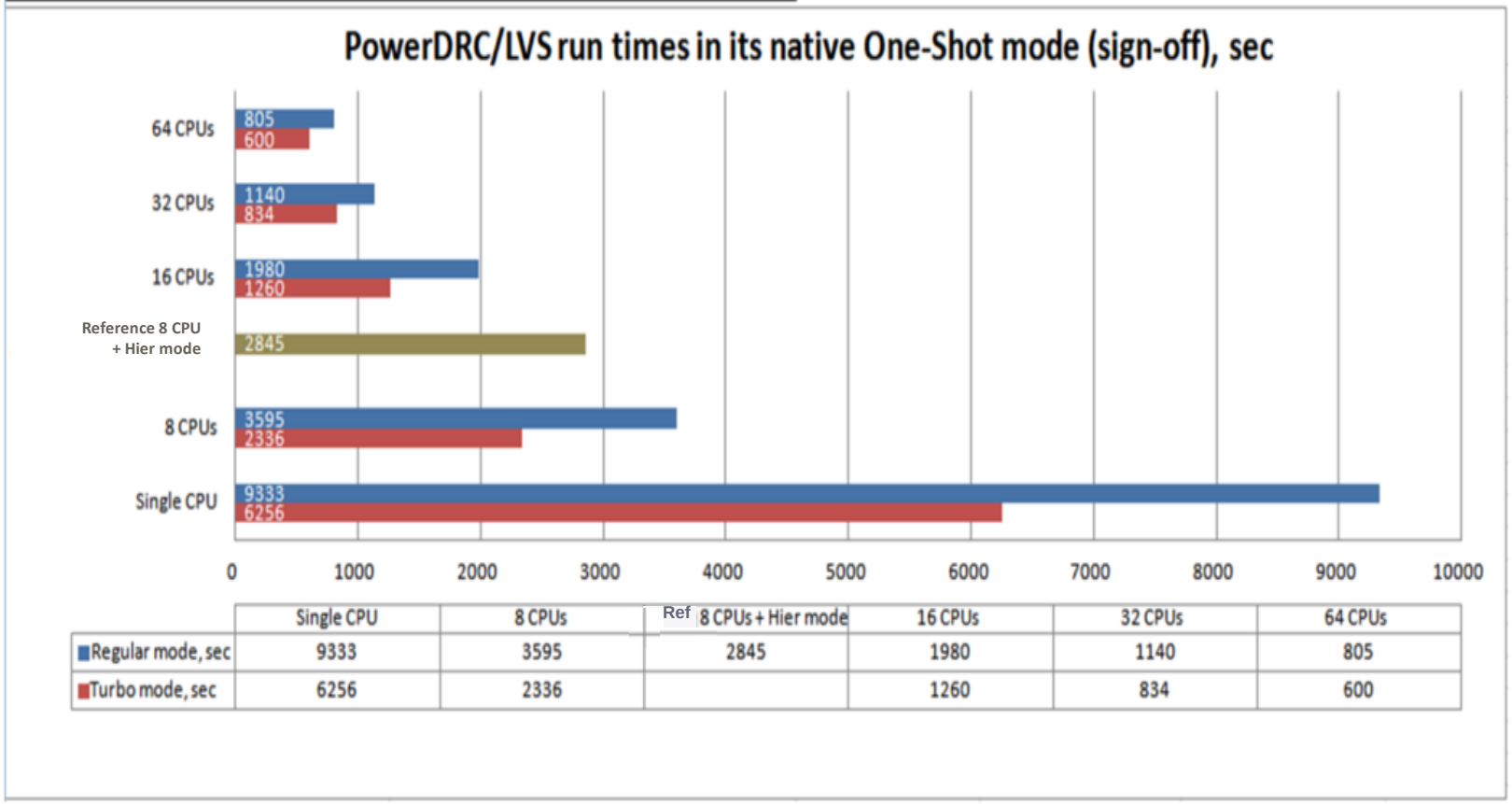
SmartDRC vs. Reference

Performance

Test name	Chip A
GDS size	660MB
Area	~45 sq. mm
Specifics	Full chip: Standard Logic + PADs + power ring
Process node	180nm, 6 metals

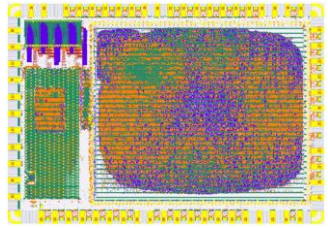
Hardware configuration: 4 x Intel Xeon E5-2686 2.3GHz (64 CPU cores), RAM: 128GB, HDD: 10GB SAS+ 150GB

Software configuration: CentOS 7 64 bit, PowerDRC/LVS version: 2.5.0



	Single CPU	8 CPUs	Ref 8 CPUs + Hier mode	16 CPUs	32 CPUs	64 CPUs
Regular mode, sec	9333	3595	2845	1980	1140	805
Turbo mode, sec	6256	2336		1260	834	600

Using the Google Open Source Caravel SOC example on 130nm Process, Smart DRC was 3X faster than a Competitor (single CPU / Flat)



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SmartLVS
Performance on Big Chips

Test name	baseband8_io	OPT ROM_512_1024_64	Flexible LCD display
LVS Mode	Hierarchical	Flat	Hierarchical + Flat + Blackbox (mixed)
Process	250 nm	130 nm logic rules	Special rules
Chip size, um	5004.1 x 9954.1	1432 x 1074	132236.110 by 161550.000
Number of devices	304,738 + 857 merged	1,091,164+ 9630 merged	405,303
Number of nets	329,656	545,655	648,889
LVS extraction time, min	16.9	1.7	2.2
Peak VM usage LVS	5,788 MB	1,112 MB	572 MB
NVN comparison time, min	10.8	3.3	1.1
Peak VM usage NVN	1684 MB	2150 MB	106 MB

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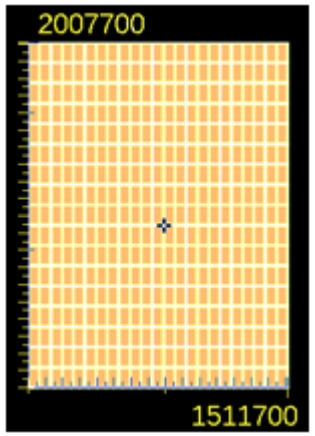
SmartLVL
Performance (1.5m x 2m) Glass Substrate

- Basic design
  - Type: panel design for smartphones
  - Size: 116.5mm * 64.1mm
  - Number of pixels: 720*1280
  - Number of layers: 17
- Rule file: auto-generated
- XOR'ed:
  - The basic design arranged as a 17 * 23 array
  - Its copy with intentionally added error



# of CPUs	Elapsed Run Time hh:mm:ss	Peak memory MB
2	4:48:43	664
4	2:46:54	668
8	1:27:41	662

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PWRL
Rule Language

- PWRL (pronounced Power-L)
- Rich set of checks and operations
- Flexible due to preprocessing tools like variables, conditionals, macros, and includes
- Easy to learn and use
- Allows for full or partial rules encryption (Silvaco's encryption library)
- Compile Only mode of SmartDRC/LVS allows for rule file debugging

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PWRL
Examples 1 (DRC)

Simple spacing rules:

```
w2bs {//@Minimum SUB_E width ... 0.5
tmp_1 = sub - dti_all;
$width tmp_1 < 0.5 $singular;//
}
s1bs {//@Minimum SUB spacing/notch ... 2.0
$space sub < 2 $singular;//
}
a1bs {//@Minimum SUB area ... 9.5
$area sub < 9.5;

}
```

Edge operations:

```
pmve_ex61 = $coincident_outside_edge
pmve_psd pmve_s2;
tmp_1 = $expand_edge pmve_ex61 $outside_by
1.09;
pmve_ex62 = pmve_psd + tmp_1;
s1bs {//@Minimum SUB spacing/notch ... 2.0
$space sub < 2 $singular;//
}
```

Density check:

```
Mett_pl_density {//@
$density [ area (mettpl) / area (bulk_dens_nll) ] <
0.30 $inside_layer bulk_dens_nllc;// METTPL

}
```

Metal fill generation:

```
M1_fill {$fill 0.6 0.6 0.2 0.2 $offset 0.4 -0.4 $shift 0.1 0.1 $outside nofill0 $prefix prefix0
$append suffix0;}
```


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PWRL
Examples 2 (LVS)

- Connectivity:
  - $connect m2trm m1trm csf_m1 $by via1 ;
  - $connect csf_m2 m1trm csf_m1 $by via1 ;
  - $sconnect ndiff ntap ;
  - $sconnect ptap bulk ;
- Text labels:
  - $attach met1_text m1trm ;
  - $attach met2_text m2trm ;
  - rpp1_3 = $with_text "rpp1_3" rpp1 polylabel_txt ;
- Device and parameters:
  - $device DIO (ds5) ds5 d_dsdf (POS) nwtrm (NEG)
  - [$property AREA PERIMETER W ;
  - AREA = area (ds5) * 1e-12 ;
  - PERIMETER = per (ds5) * 1e-6 ;
  - W = AREA / 0.94e-06] ;

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PWRL vs. SVRF

Very Similar, Yet Different

- You cannot get PWRL from SVRF by mere substitution of keywords
- SVRF: arbitrary order of commands in the rule files, PWRL: strict order
- No direct SVRF equivalents, e.g., for PWRL's **block** or **$via_enclosure**
- Likewise, no direct PWRL equivalents for some SVRF commands
- Multiple differences in **$net_parameter** cp. **NET RATIO** for antenna rules
- And on, and on...

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PWRL
Pre-Advanced Nodes

Special PWRL commands for advanced process nodes

Runs much faster than comparable rule code in other products

- $line_end –access complex geometry easily with less code lines (part of DFM rules)
- $parameter - custom devices parameters extraction (part of DFM rules)
- $net_parameter – is much better than Calibre`s NET RATIO for antenna rules
- $cluster – checks via spacing + clusters via into proximity groups
- $via_enclusure – via rule distances are measured from via edges and are sequentially applied clockwise to produce 8 orientations. No analog in Calibre

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Foundry Support
Rule Decks

- As PolytEDA
  - 10 Signoff decks from 40nm to 500nm from 6 foundries
    - Working to recertify these signoff decks

Sign-Off	UMC	Tower Semiconductor	ihp	XFAB	Silanna Semiconductor
	40nm (G, LP) **65nm** (LL, LP, SP) **180nm**(G, LL)	**180nm** TS18 (SL, PM, RF, IS)	**250nm** (SGB25V, SGH24H4) **130nm** (SG13S/G2)	**180nm** (XH018, XS018) **350nm** (XH035, XA035)	**250nm** **500nm** (GX, FX)

- As Silvaco >70 processes supported from 10+ foundries
  - 3 Signoff decks (XFAB), 5 in process (XFAB, Tower, IHP)
  - Rule decks starting at 40nm
  - Expect to be able to handle down to 28nm
- Goal
  - Support more foundries and support more 28-90nm processes (including encrypting if needed)
  - Add more support for DFM and Advance Nodes

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Rule Deck Support

Our Rule Deck focus is:

- 40nm and above
  - Should be able to handle 28nm
  - Below 28nm, colorization and FinFET extensions are required
    - Roadmap plans
- Tier 2 Foundries
  - AMS, Dongbu, IHP, On-Semi, SkyWater, Tower, Vanguard, Xfab, Others TBD
    - Prefer to do all/most processes of a foundry vs more foundries
- Can do any foundry with 3-way NDA
  - E.g., TSMC, Global Foundry, UMC, ….

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Available Decks

Foundry	Process	Node (nm)
AMS	AC18	180
AMS	AH18	180
AMS	S35	350
Dongbu	1533IL11SI	110
Dongbu	1533IL11SJ	110
Dongbu	1533IL13SH	130
Dongbu	1830AN18BA	180
Dongbu	1830BL18BA	180
Dongbu	1833IS18SI	180
Dongbu	5045BD18BA	180
HHGrace	gsmc-f013q7pr	130
HHGrace	hhgrace-bd500hc1c	500
HHGrace	hhnec-bcd350	350
IHP (new)	SG13G2-AI	130
IHP (new)	SG25H5-EPIC	250
IHP (new)	SG25V_H4	250
Lapis (IBM) (new)	180nm	180
On Semi	ONC18	180
On Semi	C3	250
On Semi	C5	600
On Semi	I2T100	700
On Semi	I3T25	350
On Semi	I3T80	350
SkyWater	C9F	90
SkyWater (new)	S130	130

Foundry	Process	Node (nm)
Tower (new)	TPS65RF	65
Tower (new)	SBL13PC	130
*Tower **(ITAR)***	*CA13SAV*	*130*
Tower (new)	CA13SC	130
Tower (new)	SBC13S3	130
Tower (new)	SBC13S4	130
Tower (new)	TS13SL	130
Tower	CA18HA	180
Tower	CA18HD	180
Tower **(ITAR)**	CA18HJ	180
Tower	CA18QH	180
Tower	CS18Q1	180
Tower	PH18MC	180
Tower	SBC18H2	180
Tower	SBC18H3	180
Tower	SBC18H3b	180
Tower	SBC18HA	180
Tower	SBC18HX	180
Tower (new)	SBC18s5J	180
Tower	TS18(SL/PM/IS)	180
Tower	BCD25MB	250
*Tower **(ITAR)***	*CA25QFS*	*250*
Tower	BC35MW (BC35X)	350
Tower	SBC35QTA (QTX)	350
Tower	SBC35QTS (QTX)	350
TSI (new)	180nm	180
TSMC (new)	130BCD	130

Foundry	Process	Node (nm)
UMC	*UMC-65LL*	*65*
UMC	*UMC-130MM*	*130*
UMC	UMC-018MMRF	*180*
Vanguard	VT015CBSP001	150
Vanguard	VT015CBSP004	150
Vanguard	VT018CMSP001	180
Vanguard	VT025CBSP005	250
Vanguard	VT025CVSP013	250
Vanguard	VT03UCVSP003	300
Vanguard	VT035MMSP002	350
Vanguard	VT050HVSP001	500
Vanguard	VT05UCUSP010	500
Vanguard	VT05UCUSP010	500
Vanguard	VT05UCUSP016	500
Vanguard	VT05UCUSP028	500
Vanguard	VT05UCUSP029	500
Vanguard	VT05UCVSP006	500
Vanguard	VT05USHSP004	500
Xfab (new)	XR013	130
Xfab	XH018	180
Xfab	XP018	180
Xfab	XS018	180
Xfab	XT018	180
Xfab	XA035	350
Xfab	XH035	350
Xfab	XO035	350
Xfab	XU035	350

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Summary
SmartDRC/LVS with SmartRDE

- Silvaco believes we have a great solution for customers at 28nm and above
  - Cost-efficient
  - Competitive performance
  - Foundry-proven
  - Customer-proven

- We would like the opportunity to solve your verification needs
  - For foundries/processes not currently supported, please work with us to add support!

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