



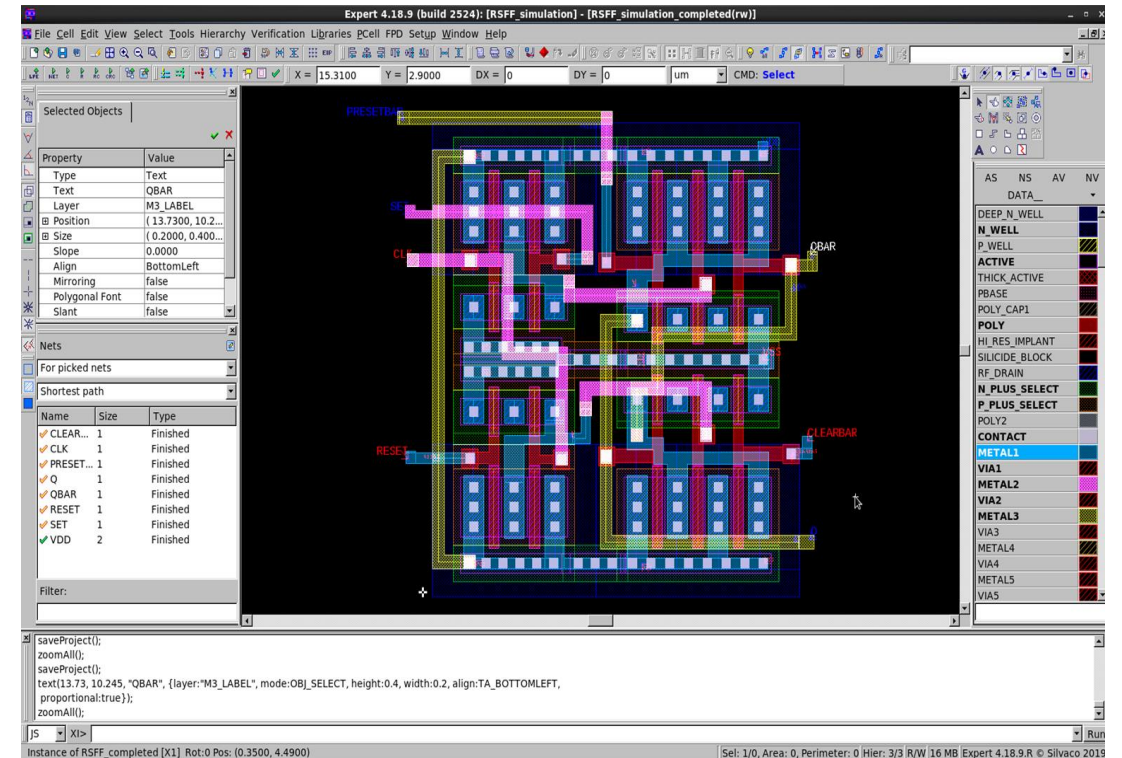
```
mirror_mod.use = False
mirror_mod.use = False
elif_operation == "MIRROR":
mirror_mod.use = False
mirror_mod.use = True
mirror_mod.use = False
elif_operation == "MIRROR_Z":
mirror_mod.use = False
mirror_mod.use = False
mirror_mod.use = True
mirror_mod.use = True
mirror_mod.use = False
#select mirror mod use and deactivate
mirror_ob.select = True
modifier_ob.select = True
bpy.context.scene.objects.active = modifier_ob
print("Selected modifier ob")
bpy.context.scene.objects.active = mirror_ob
print("Selected mirror ob")
#please select exactly two objects, the last one gets the
```

SILVACO

Expert Layout Editor

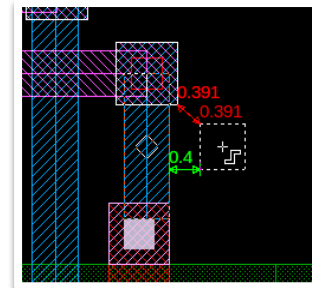
Expert Overview

- Full feature, custom layout editor
- Customizable menus, and GUI
 - Toolbars
 - Panels
- Powerful Java scripting capability
- Productivity features
 - DRC Assist
 - Edit-In-Place
 - Connectivity highlighting
 - Short locator
 - Embedded Layout vs Layout
 - Flat Panel Display Features
 - Cross-sectional Viewer
- OpenAccess and iPDK Support
- API for external control via Python scripts

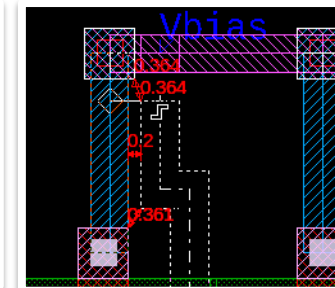


Expert DRC Assist

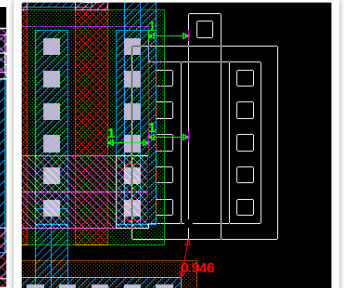
- Shows violations while editing layout design in real-time
 - Shows flags for the starting point
 - Works with various editing commands
 - Recognizes shapes through hierarchy
- Works with basic design rules
 - All rules are kept in the technology file
- Shows resistance of wire currently being created



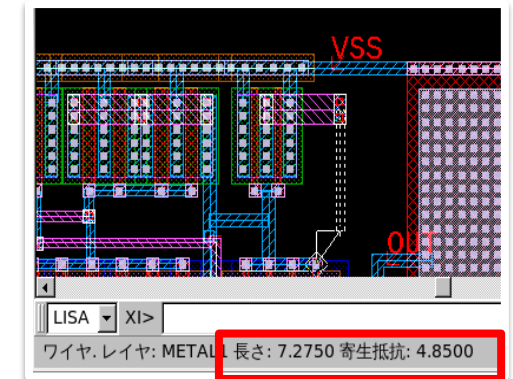
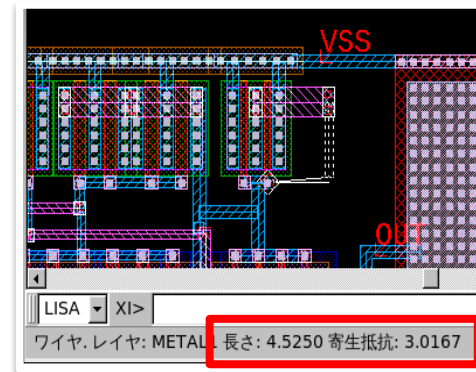
Recognizes the violation along cursor before starting



Shows error flags with numeric information



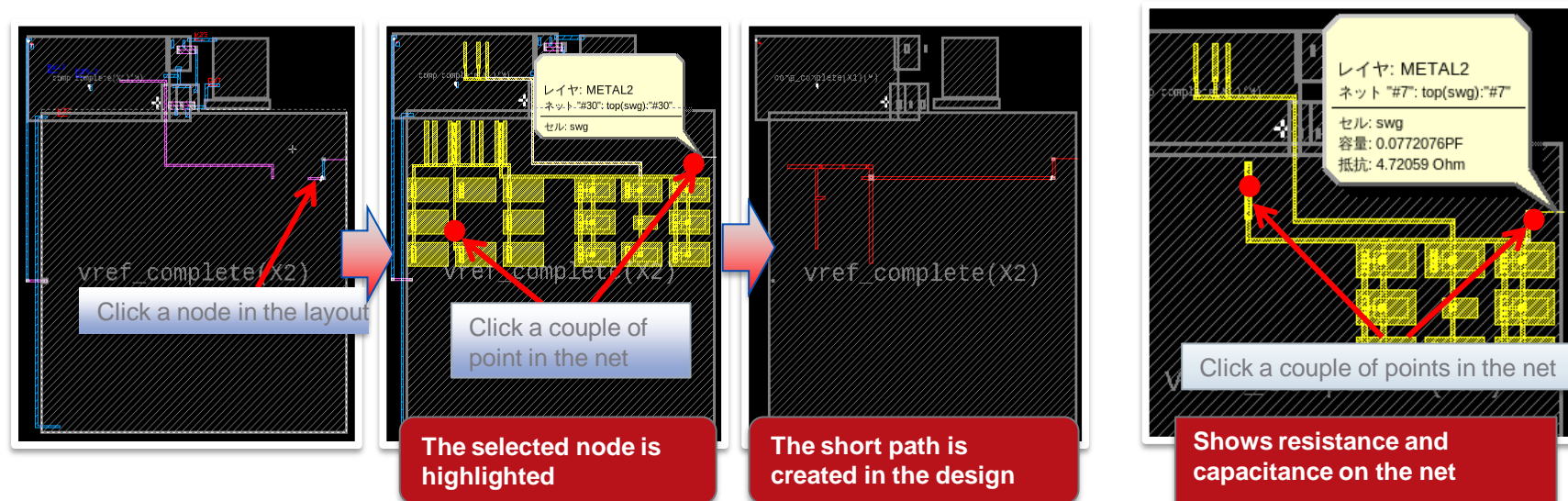
Recognizes shapes in lower cells



Expert

Node Probing

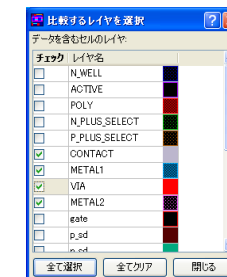
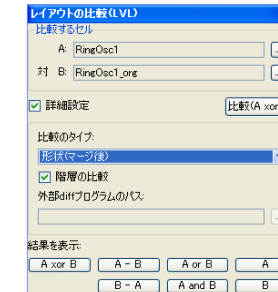
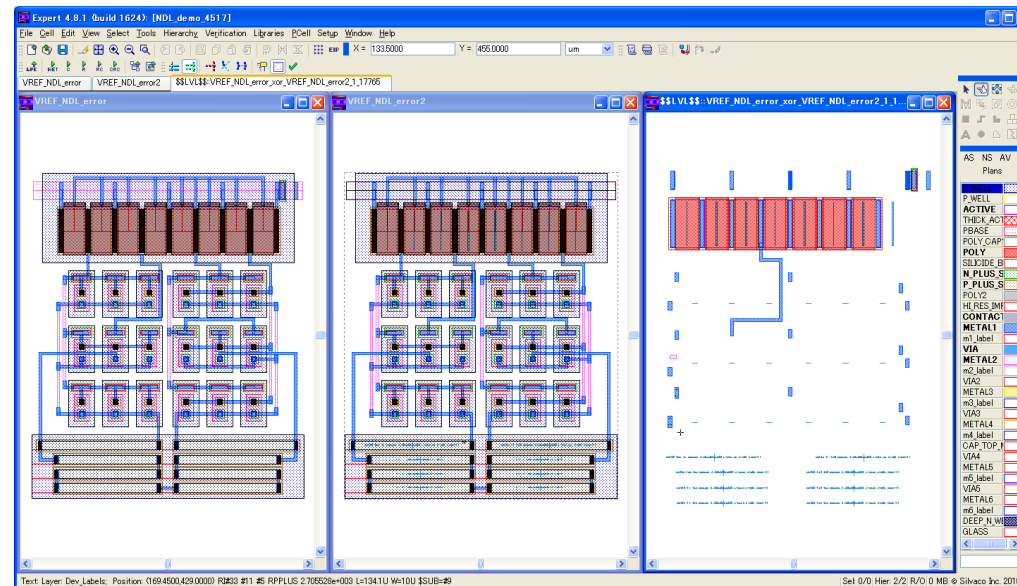
- Shows electrically connected path with layer connectivity information
- Performs hierarchical processing for fast extraction even in a large design
- Short-locator
- Especially effective to find short between power and ground nets
- Shows resistance value between a couple of specific points calculated by Hipex



Expert Layout Comparison

Layout comparison (LVL = Layout vs. Layout)

- Compare two layouts
 - Show the result of AND, OR, Dif (=Not), and XOR
 - Creation of text report
 - Can restrict comparison to specific layers

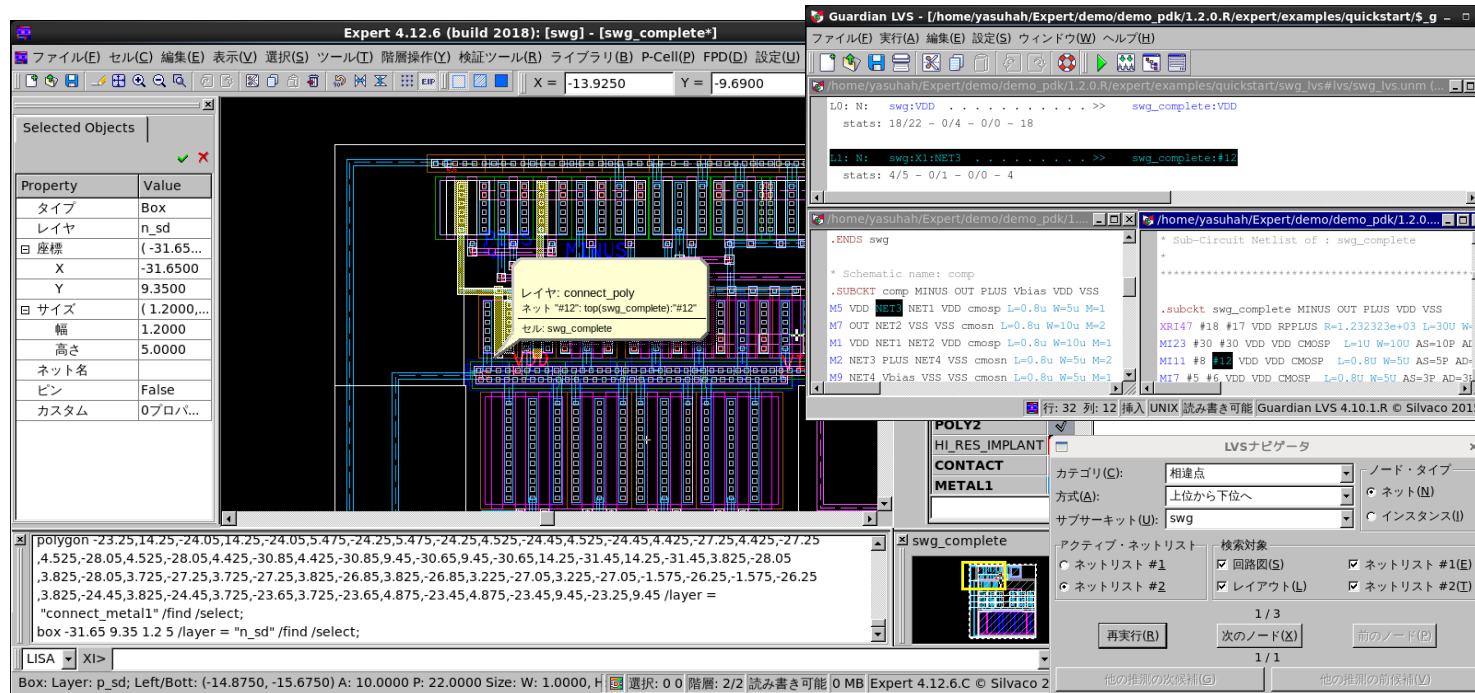


Expert

Integration with Gateway Schematic Capture

Cross-probing with Expert and Gateway

- LVS navigators provide various comparison information
- Provides cross-probing between Expert, Gateway and SmartDRC/LVS

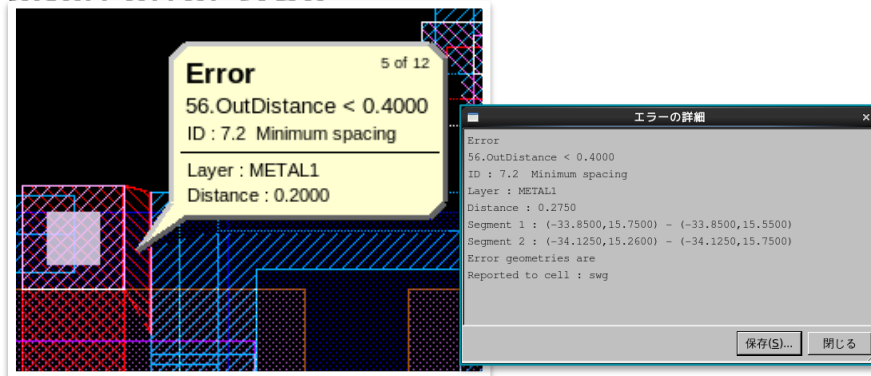


Integration with Guardian DRC

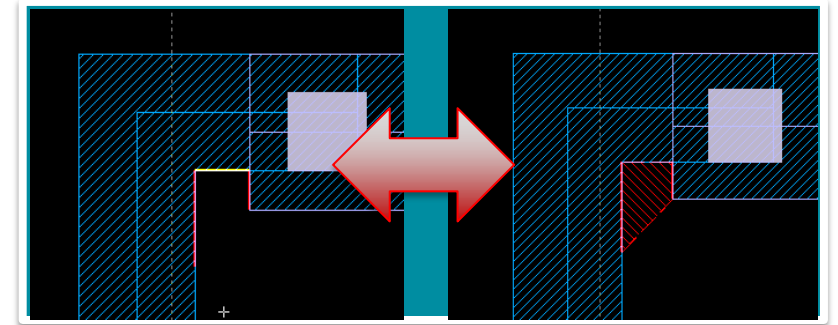
Integration with SmartDRC

Finding detected errors in SmartDRC

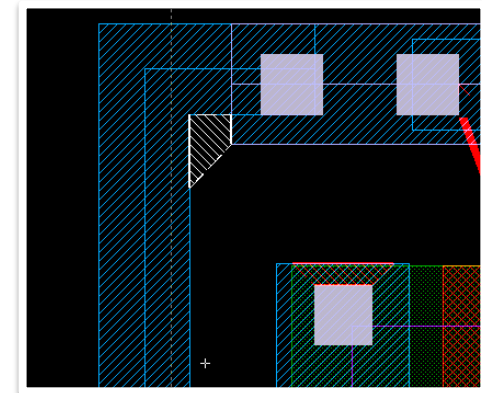
- Shows details in bubble mark
- Can switch style of error flags
- Shows Next / Previous / First error
- Shows errors in fixed window
- Allows setting color for each error type



Showing detailed information



Various style of error flags



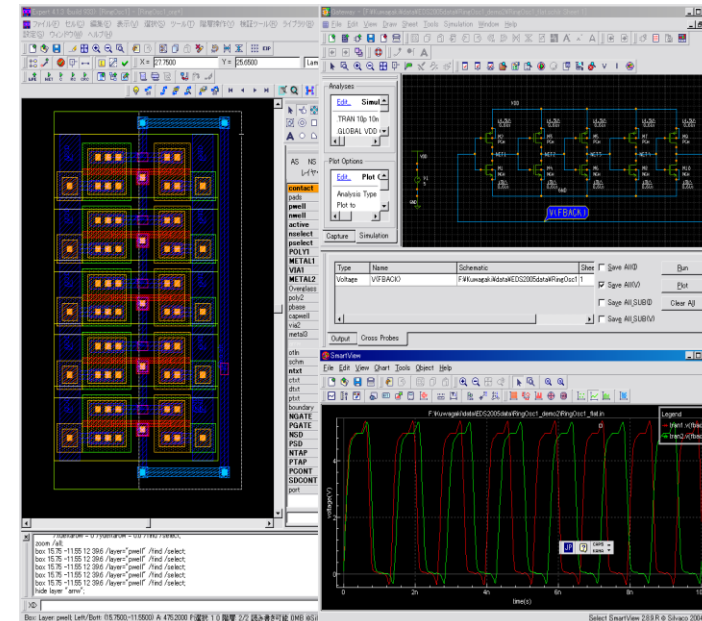
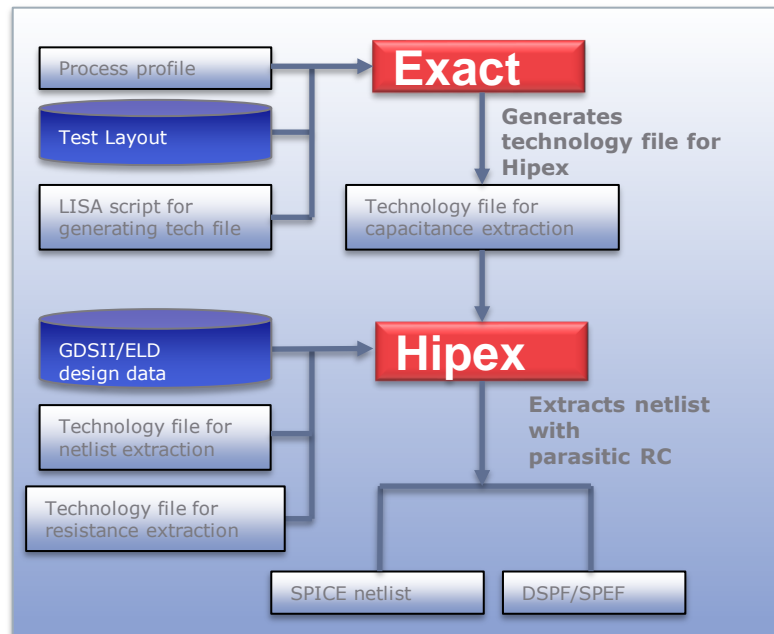
Allows setting color for each error type

Expert

Integration with Hipex

Fast and Accurate Parasitic Extraction

- Tightly bound with Expert and SmartLVS
- Back-annotation to schematic netlist

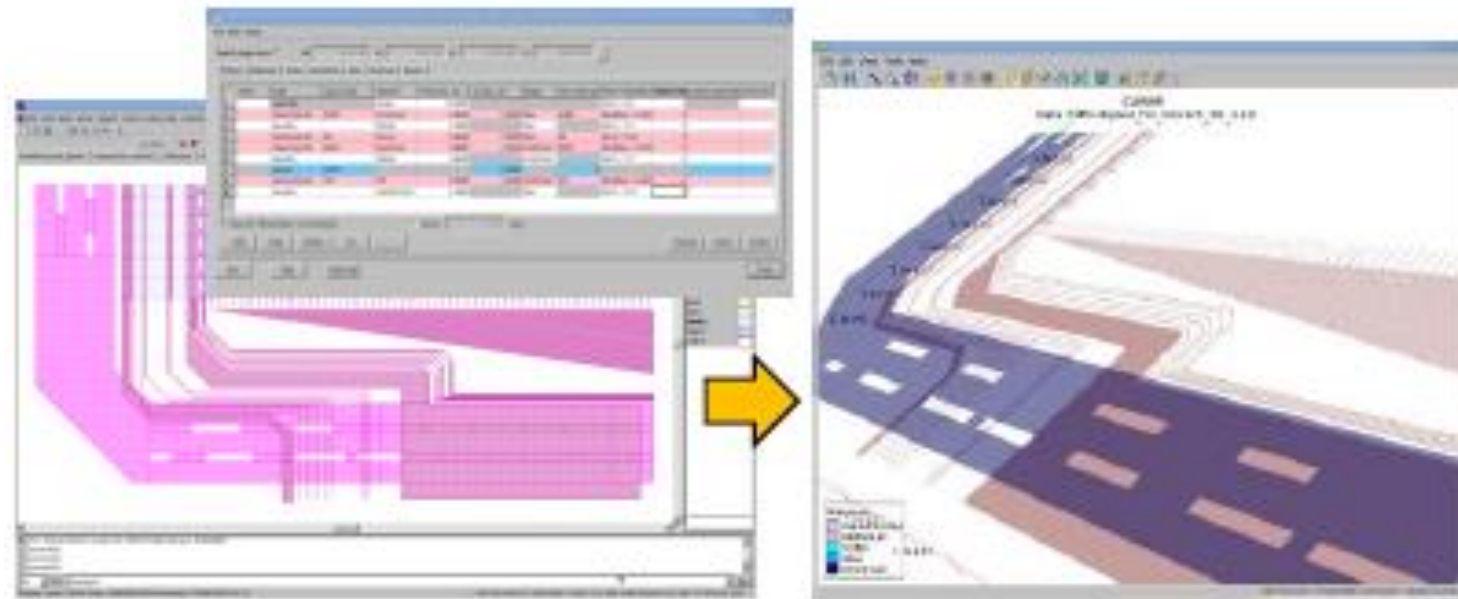


Integration with Clever

Integration with Victory RCx Pro

Victory RCx Pro

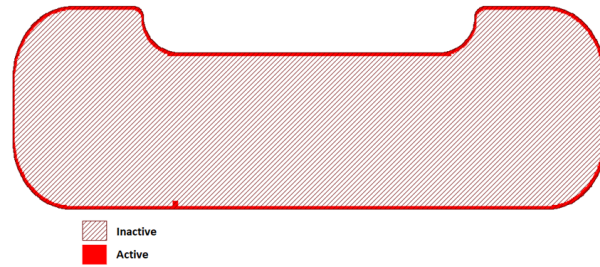
- Accurate capacitance extraction using 3D field solver
- Uses text labels to create electrodes in Clever
- Provides a feature to add text to all floating nodes automatically



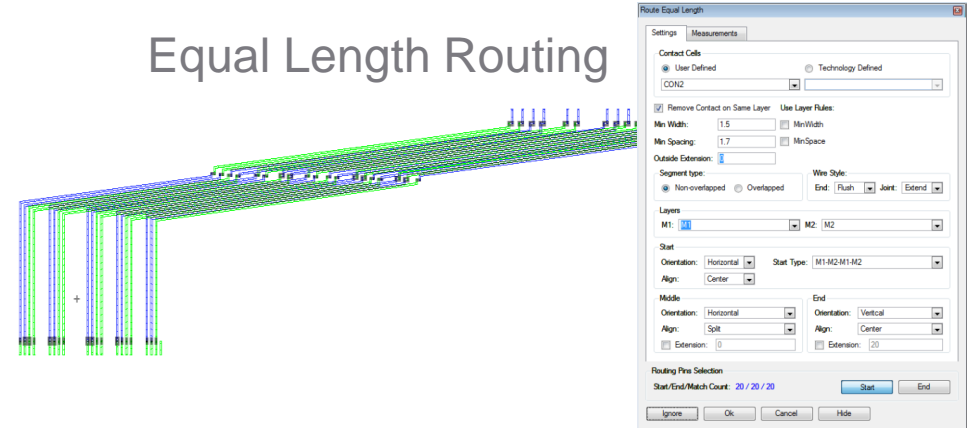
Expert Flat Panel Display Features

Extensive FPD features

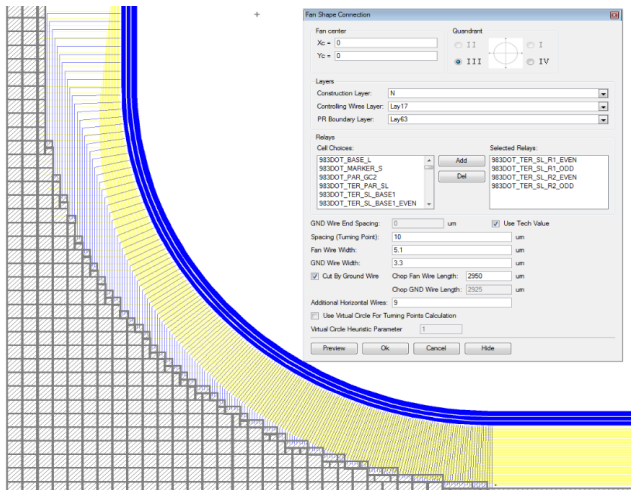
Smart Array Filtering in DRC



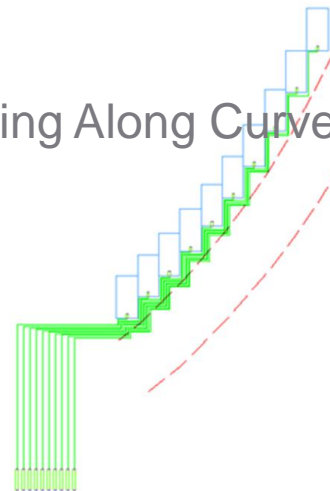
Equal Length Routing



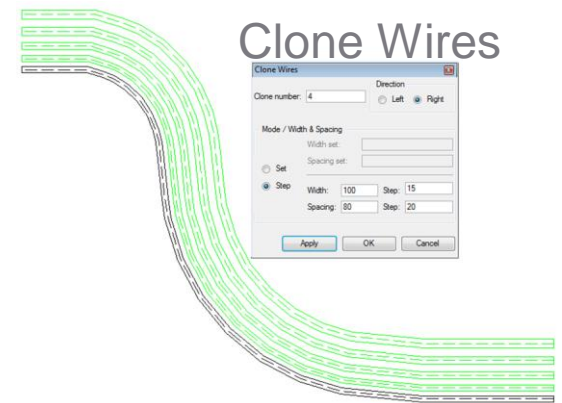
Fan Shaped Connections



Routing Along Curve



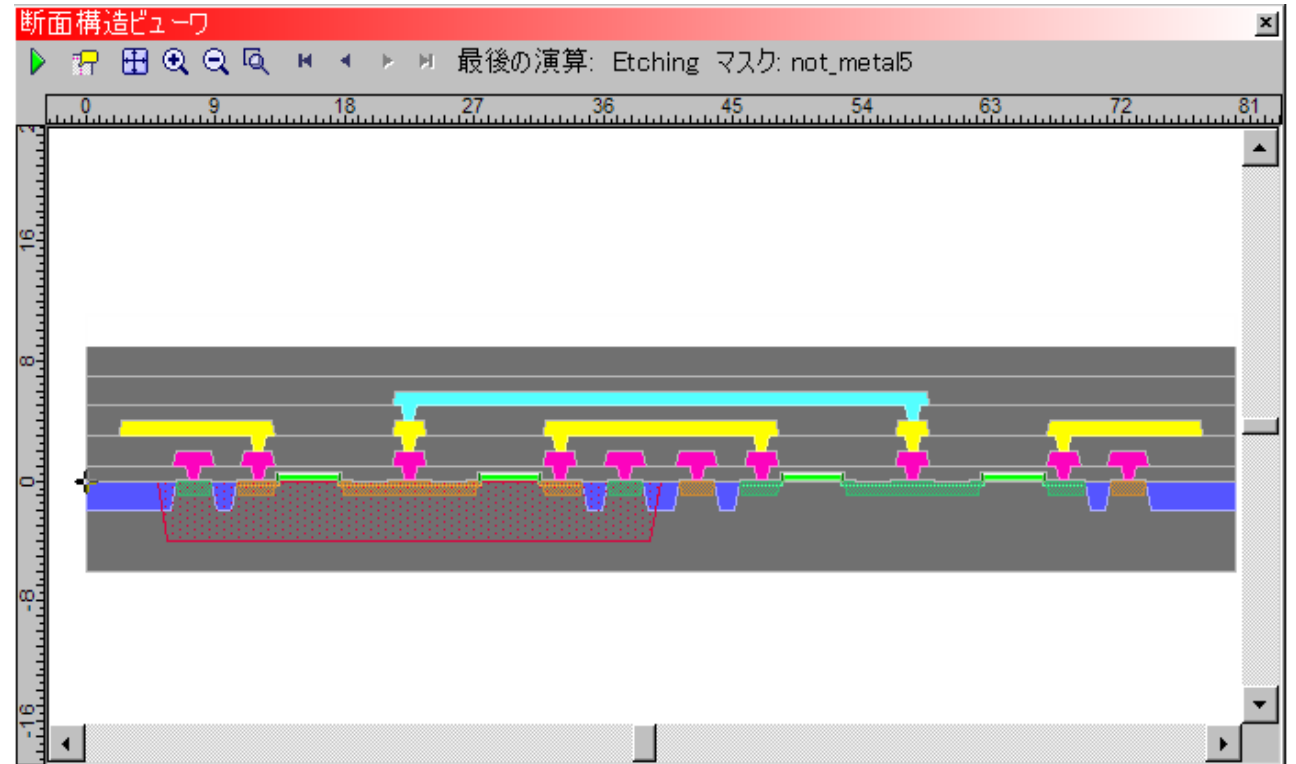
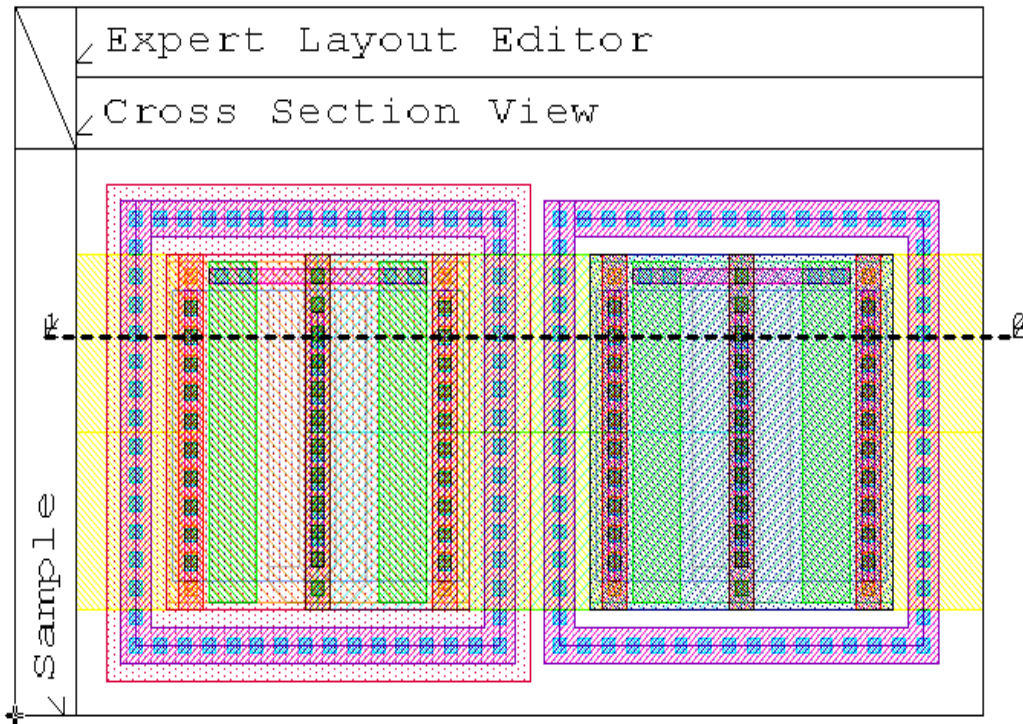
Clone Wires



Expert Viewer

Cross-sectional Viewer

- Creates the cross-sectional view of entered cut-line in the layout



Expert Summary

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