



```
mirror_mod.use = False
mirror_mod.use = False
elif operation == "MIRROR":
    mirror_mod.use = False
    mirror_mod.use = True
    mirror_mod.use = False
elif operation == "MIRROR_Z":
    mirror_mod.use = False
    mirror_mod.use = True
    mirror_mod.use = False
    mirror_mod.use = True
    mirror_mod.use = False
    #select mirror_mod.use and deselect mirror_mod.use
mirror_ob.select()
modifier_ob.select()
bpy.context.scene.objects.active = modifier_ob
print("Selected", modifier_ob)
modifier_ob.select()
bpy.context.scene.objects.active = modifier_ob
print("Selected", modifier_ob)
#please select exactly two objects, the last one gets the
```

**SILVACO**

# DTCO Integrated Tool Flow

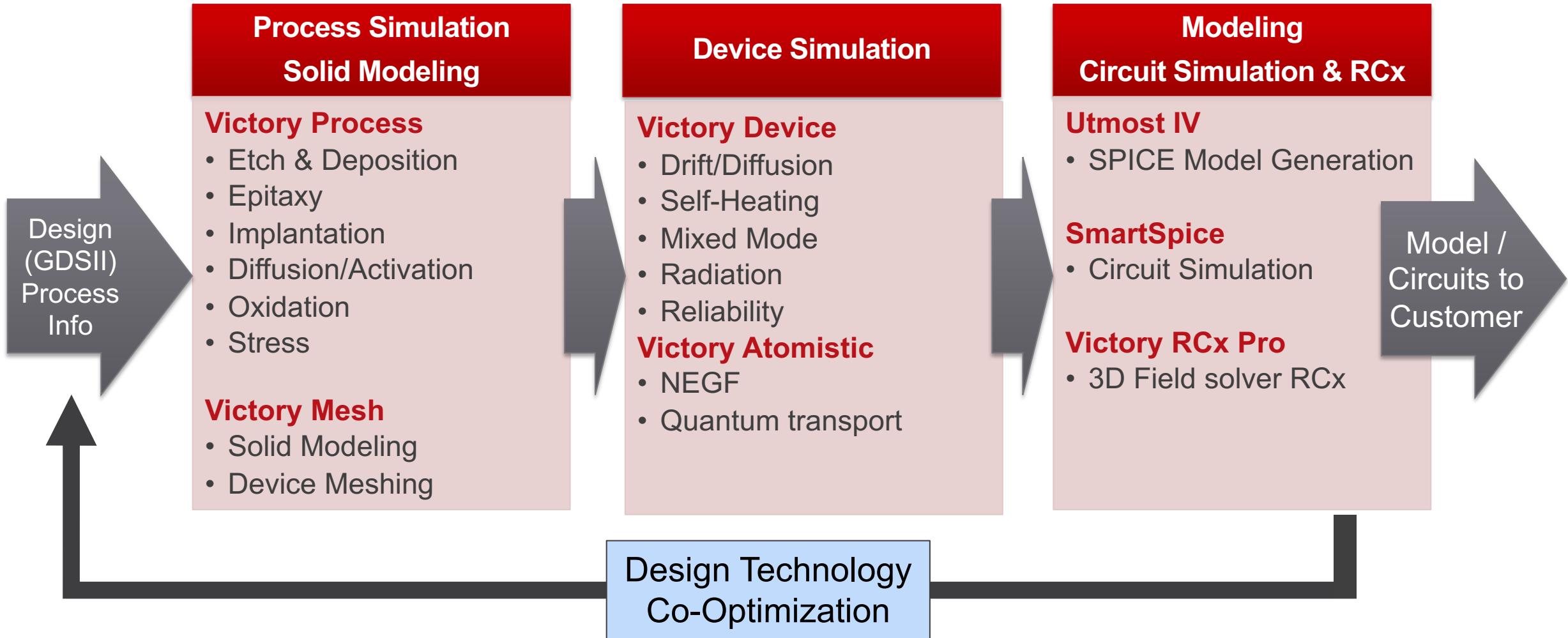
Single Run Time Environment

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# Introduction

## DTCO: Connecting Semiconductor Physics to Circuit Design

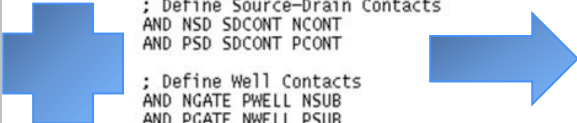
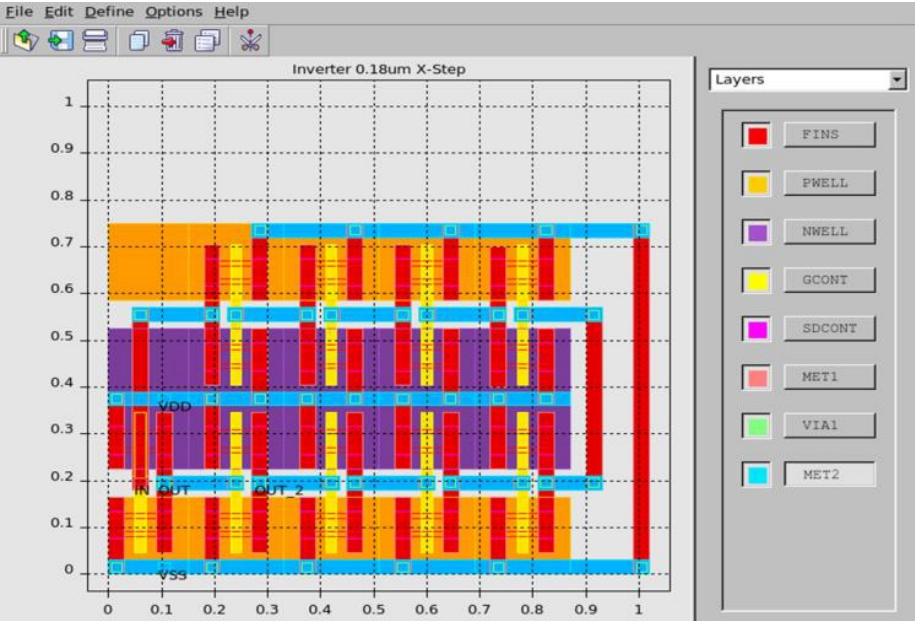


# Introduction

- Design Technology Co Optimization (DTCO) improves designs across multiple domains.
- 3D active device and BEOL parasitic extraction builders are now integrated and share the same:
  - Layout tool
  - Structure builder
  - Structure mesh generator
  - Rule file
  - Simulation interface
  - Syntax
- A single input file can now run a full TCAD to SPICE flow, enabling a powerful integrated DTCO environment

# Select Cell and Annotate using Rule File

- Supplied layout with basic labels ( Vss , Vdd , In, )
- Layout automatically annotated using the rule file



```

; Locate N and P Devices
AND PWELL FINS NFET
AND NWELL FINS PFET

; Define Gate Contacts
AND NFET GCONT NGATE
AND PFET GCONT PGATE

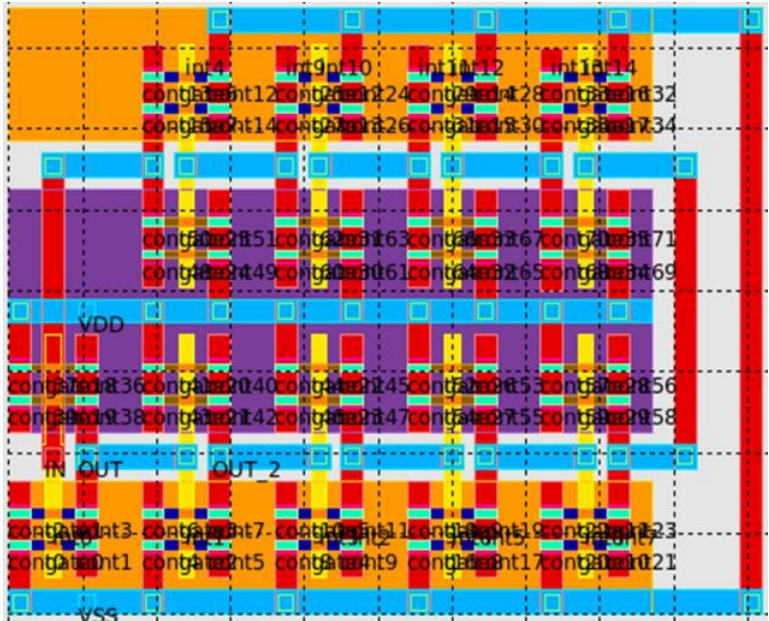
; Define Source-Drain Regions
AND NFET INGATE NSD
AND PFET IPGATE PSD

; Define Source-Drain Contacts
AND NSD SDCONT NCONT
AND PSD SDCONT PCONT

; Define Well Contacts
AND NGATE PWELL NSUB
AND PGATE NWELL PSUB

; Mask required for process simulation
OR MET1 GCONT SAC_POLY

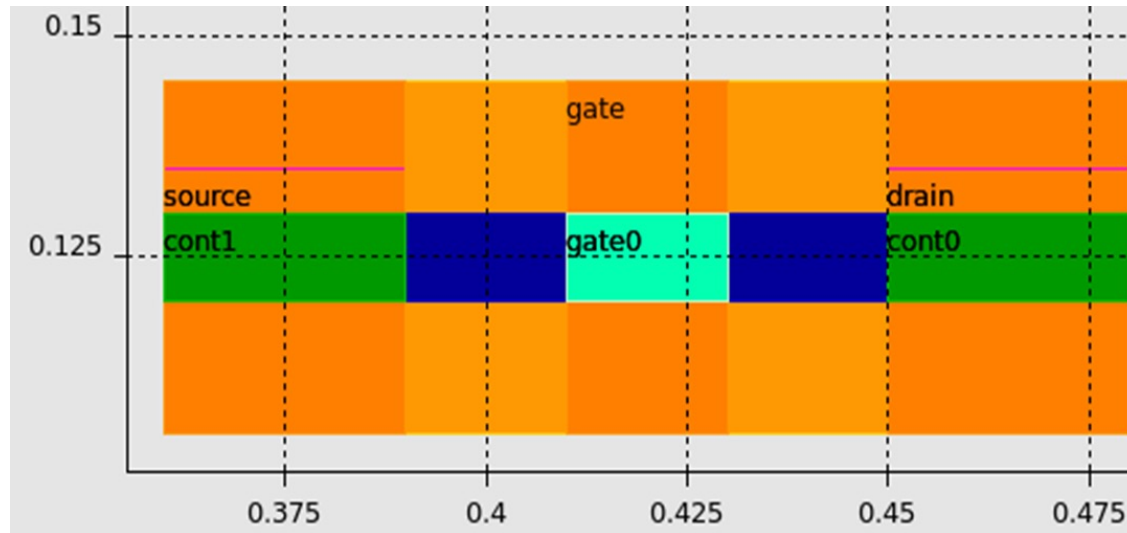
Export NGATE
Export PGATE
Export NSD
Export PSD
Export NCONT
Export PCONT
Export NSUB
Export PSUB
Export SAC_POLY
    
```



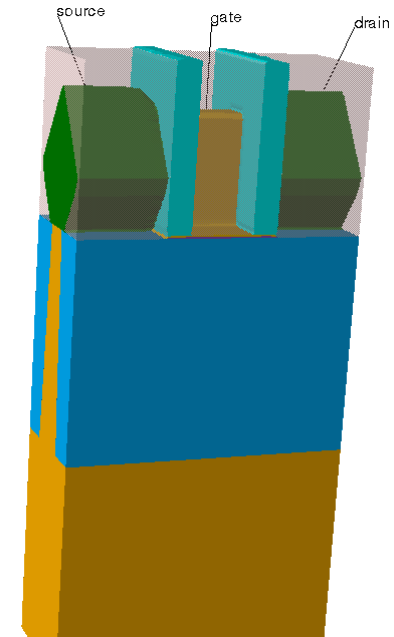
Example using a ring oscillator circuit

# Clip Layout to Build Active Devices

- From same layout, clip areas to build active devices
- Full Victory Process simulation capability available



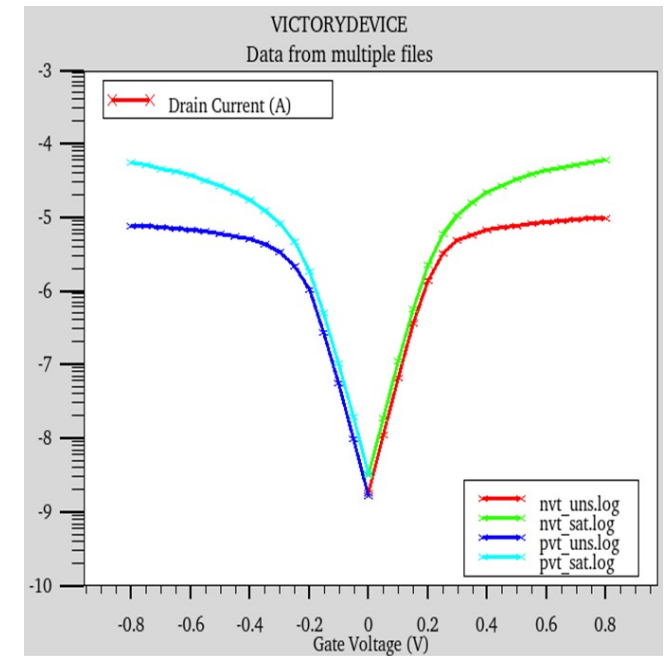
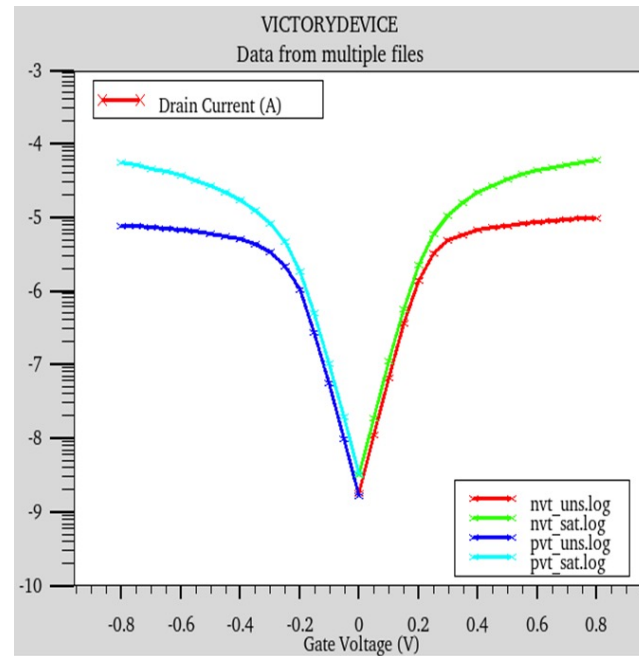
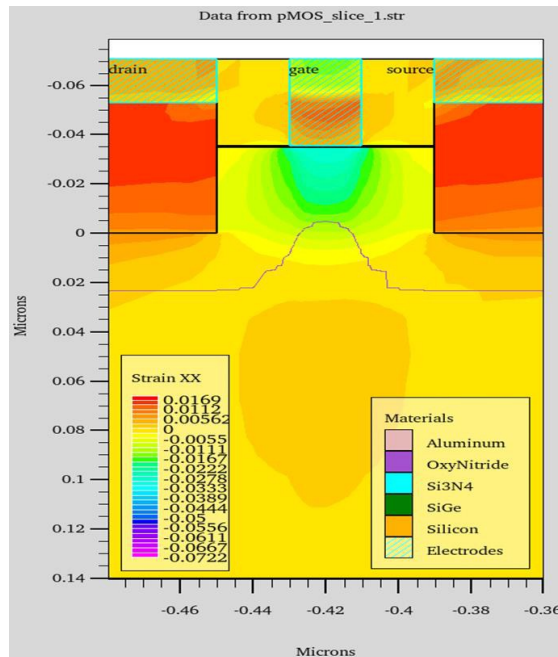
- Variables are used to automatically mesh the active structures



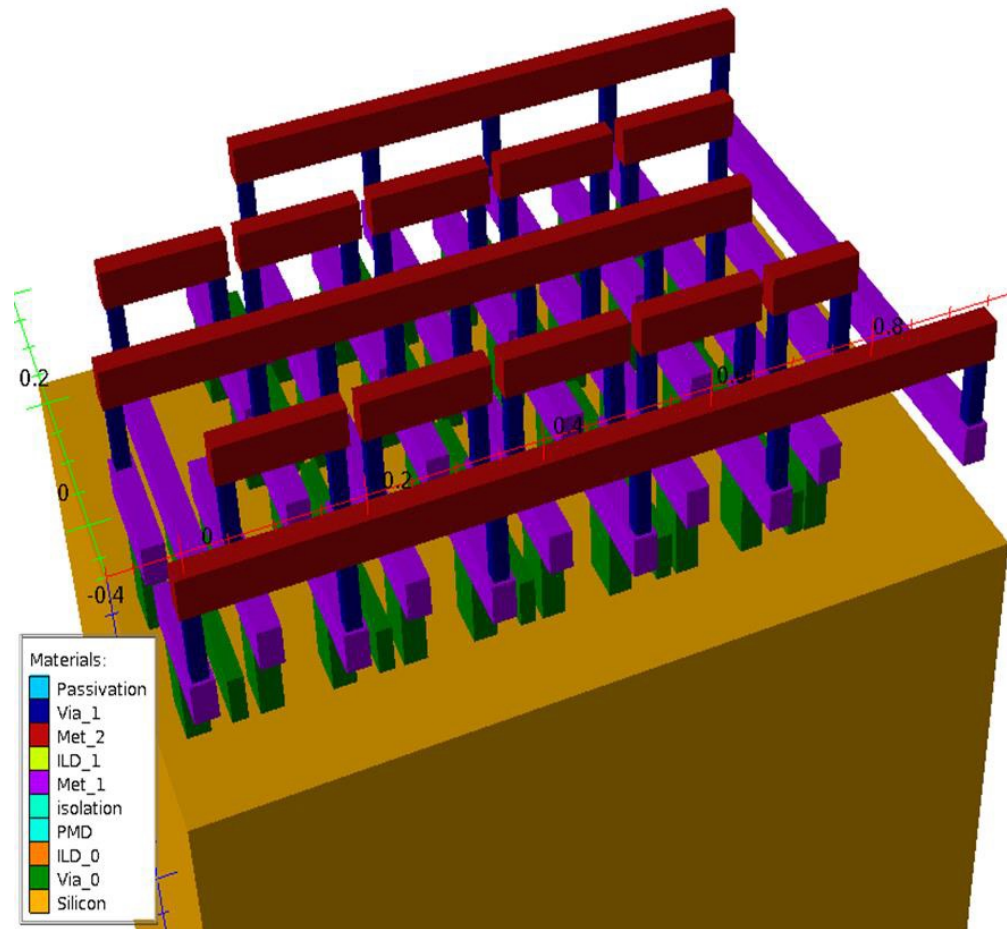
Example of stained SiGe extensions for pMOS

# Device Simulation and SPICE Model Extraction

- Simulate active device I V and capacitance curves
- Automated multi gate SPICE model extraction



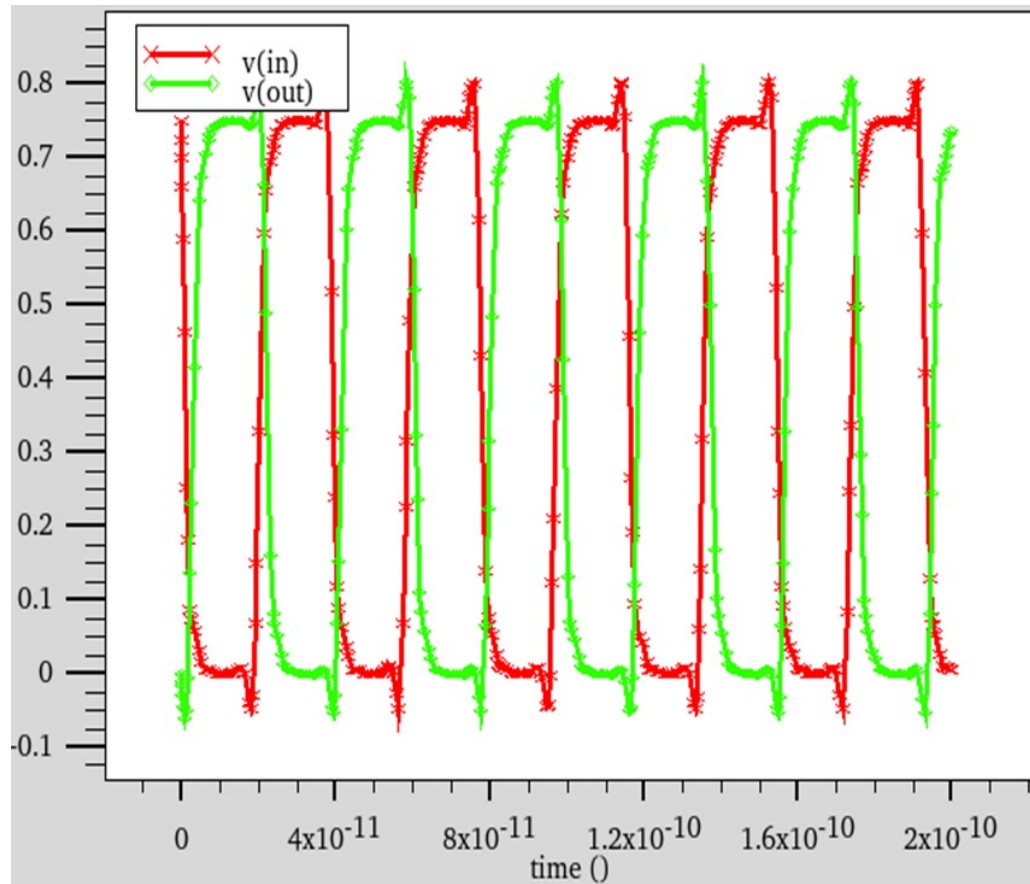
# 3D BEOL Structure for RCX Field Solver



- A Full 3D structure is created for BEOL field solver
- Active device netlist automatically extracted, then
- RC parasitics extracted and automatically back annotated
- Same structure builder/syntax as used for active devices



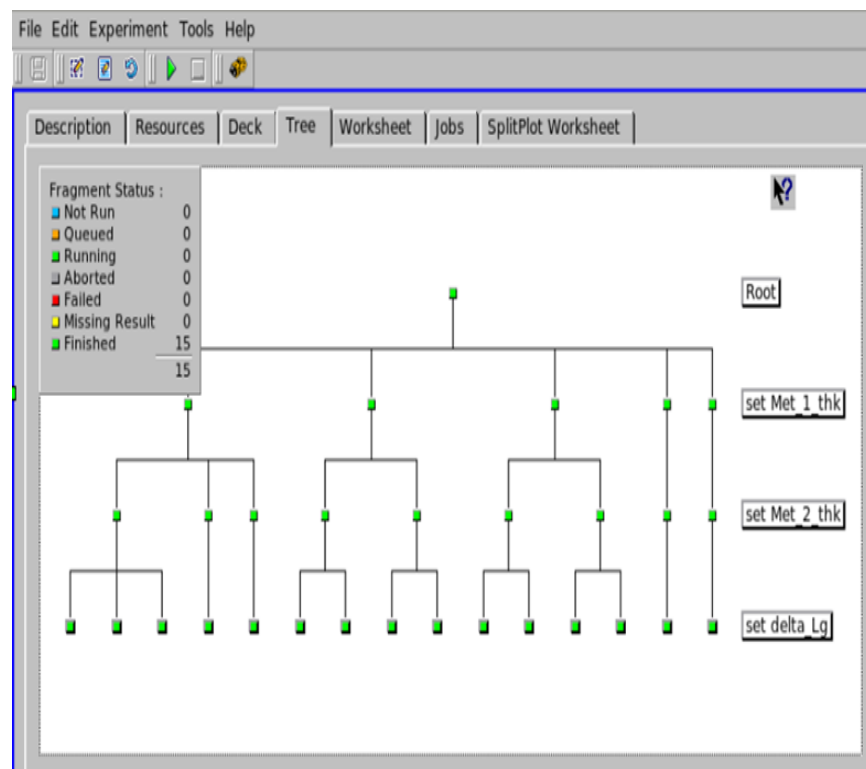
# SPICE Simulation within Same Input File



- Use “.INCLUDE” statement in SPICE to import created netlist
- SPICE simulations run and key performance parameters extracted for full flow optimization
- All run using the same interface and script

# DTCO Statistical Analysis Environment

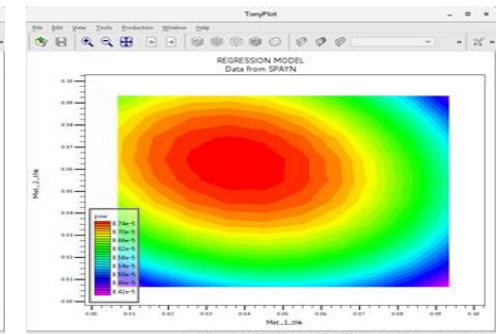
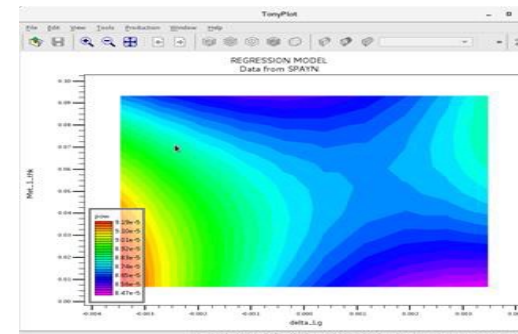
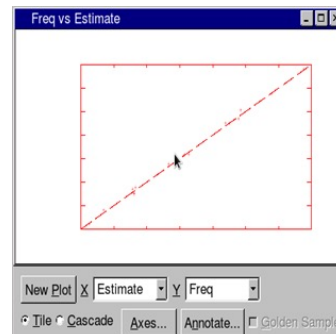
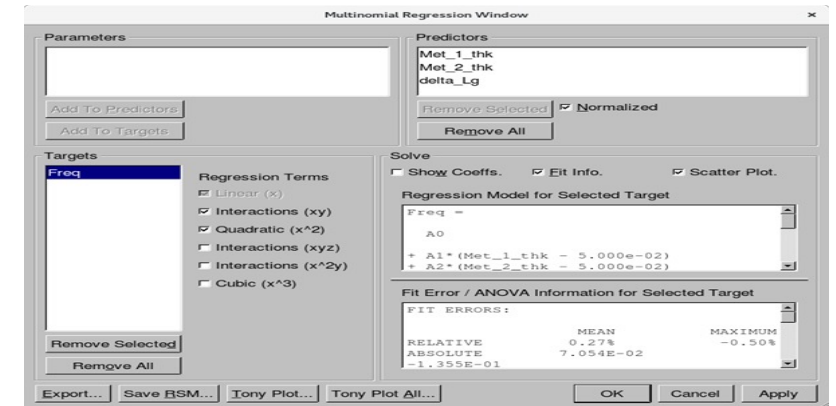
- Design of Experiments and analysis environment
- Statistical analysis of layout/process/circuit dependencies



Spain

|    | Met_1_thk | Met_2_thk | delta_Lg   | pow       | Freq      |
|----|-----------|-----------|------------|-----------|-----------|
| 1  | 5.000e-02 | 5.000e-02 | 0.000e+00  | 8.723e-05 | 2.600e+01 |
| 2  | 5.000e-02 | 5.000e-02 | 3.464e-03  | 8.609e-05 | 2.483e+01 |
| 3  | 5.000e-02 | 5.000e-02 | -3.464e-03 | 9.129e-05 | 2.733e+01 |
| 4  | 5.000e-02 | 9.330e-02 | 0.000e+00  | 8.727e-05 | 2.498e+01 |
| 5  | 5.000e-02 | 6.700e-03 | 0.000e+00  | 8.406e-05 | 2.692e+01 |
| 6  | 2.500e-02 | 2.500e-02 | -2.000e-03 | 8.995e-05 | 2.853e+01 |
| 7  | 2.500e-02 | 2.500e-02 | 2.000e-03  | 8.568e-05 | 2.692e+01 |
| 8  | 2.500e-02 | 7.500e-02 | -2.000e-03 | 8.804e-05 | 2.706e+01 |
| 9  | 2.500e-02 | 7.500e-02 | 2.000e-03  | 8.780e-05 | 2.571e+01 |
| 10 | 7.500e-02 | 2.500e-02 | -2.000e-03 | 8.627e-05 | 2.601e+01 |
| 11 | 7.500e-02 | 2.500e-02 | 2.000e-03  | 8.739e-05 | 2.501e+01 |
| 12 | 7.500e-02 | 7.500e-02 | -2.000e-03 | 8.641e-05 | 2.483e+01 |
| 13 | 7.500e-02 | 7.500e-02 | 2.000e-03  | 8.633e-05 | 2.393e+01 |
| 14 | 9.330e-02 | 5.000e-02 | 0.000e+00  | 8.613e-05 | 2.436e+01 |
| 15 | 6.700e-03 | 5.000e-02 | 0.000e+00  | 8.550e-05 | 2.782e+01 |

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# Summary

- Single fully integrated run time environment
- Anything can be a variable Layout, Process, BEOL
- Clear actionable results for Design Optimization
- Complete and full TCAD to SPICE simulation capability
- Parameterization models linking all design variables
- Powerful extract statements for parameter extraction
- All tools developed in house for smooth integration
- Worldwide support for your success