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FROM ATOMS TO SYSTEMS

Parasitic Extraction
Clever and Hipex-FS

Integrated Full Chip and Cell Level RCX

Combine Rule Based and Field Solver Solutions

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Introduction

- Many Solution Methodologies Exist for RCX Extraction
- No One Methodology is Suitable for all Circuit Blocks
- Combine Solution Methods for each Cell or Block
- Common Integrated Platform to Localize User Options
- Consider Intended User Skill Set, CAD versus TCAD
- Consider Size and Topology, versus Simulation Speed
- How Much Accuracy do you Really Need ?
- User Choices are Often Technology Dependent

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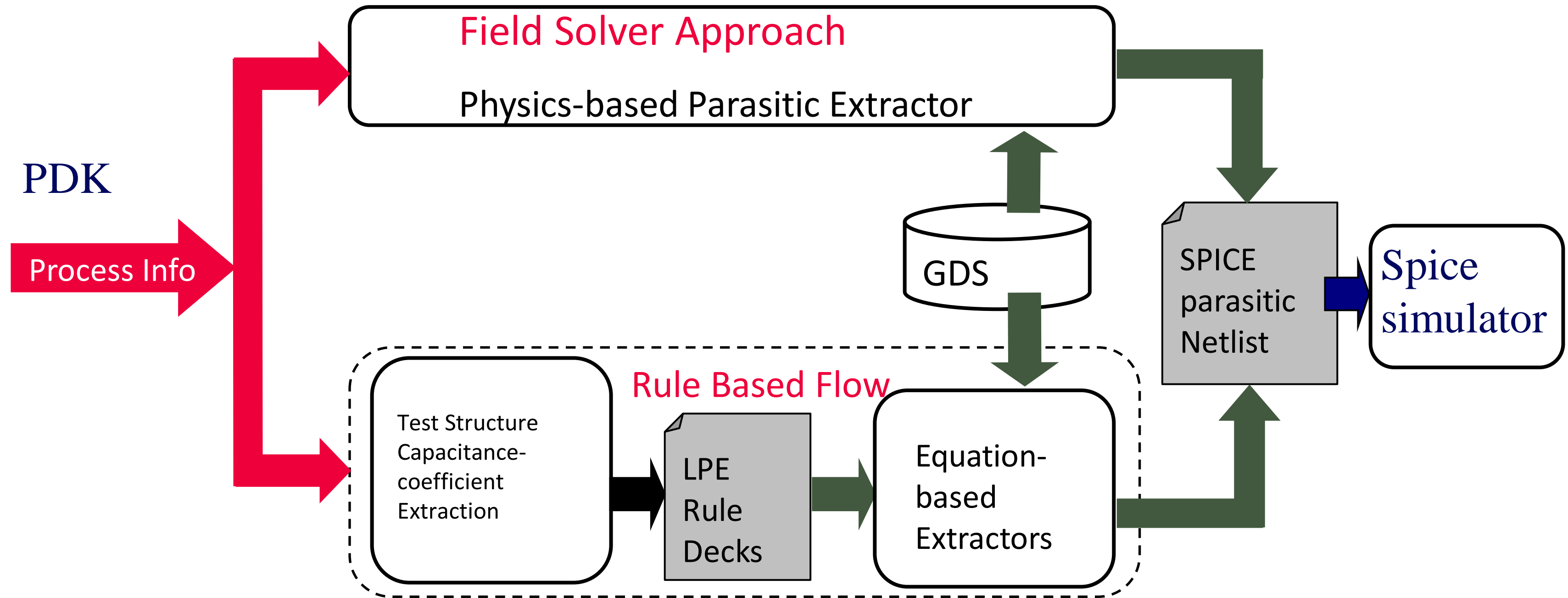
Solution Methodologies

- Rule Based - or - Field Solver Based



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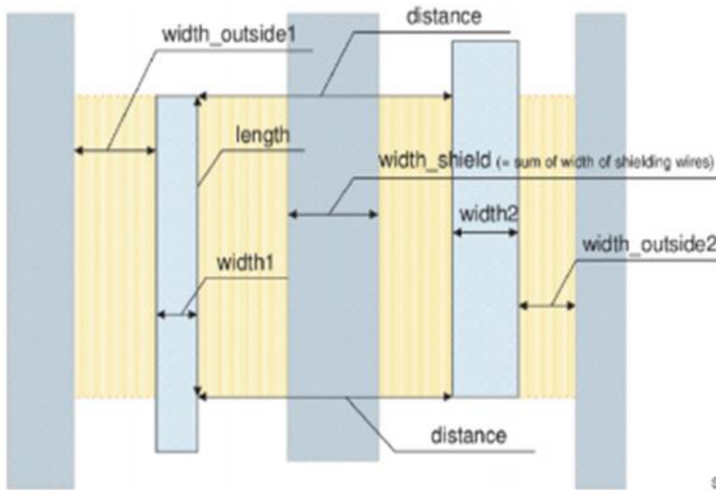
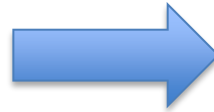
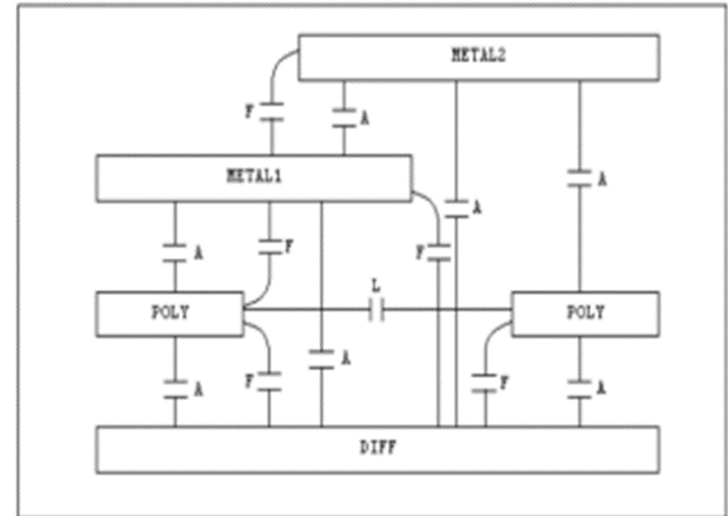
Rule Based

- Capacitance – Extract Geometry from layout Polygons
- Resistance – Count Conductor Length in “Squares”
- Coefficient Database Converts Polygons into C and R







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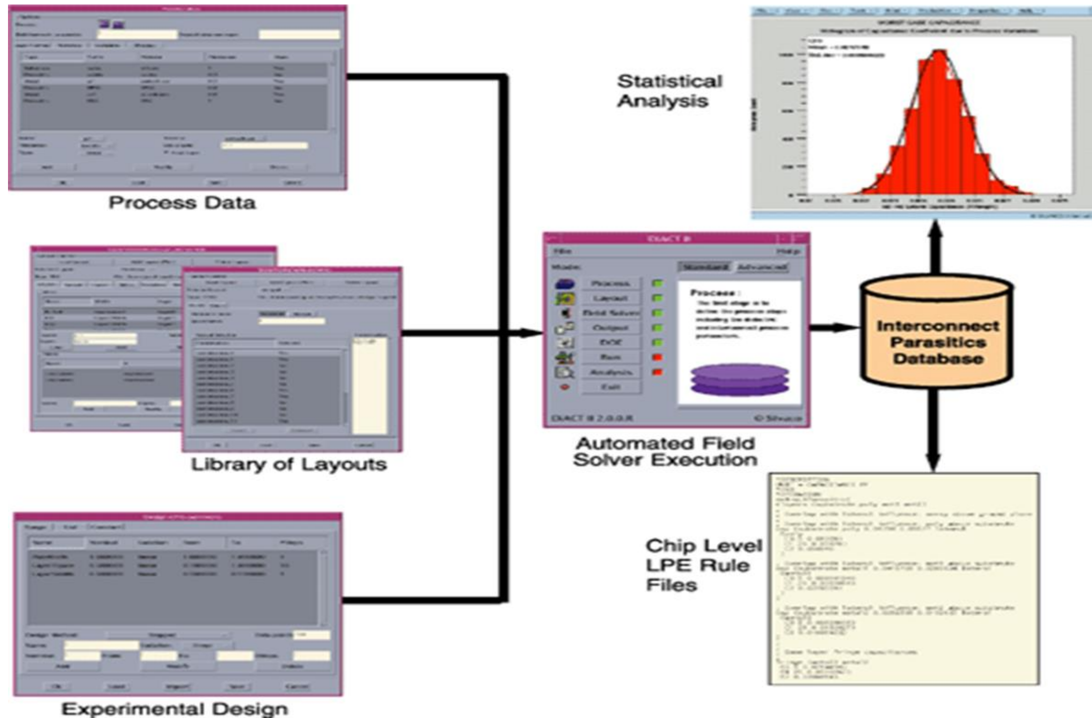
Generating Parasitic Database



- However, generating the large capacitance coefficient database for rule-based extraction, also requires a specific field solver solution, one time per technology

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Field Solver Methods

- Field Solver’s have several methods to apply the physics to the Physical Representation of the Structure
- Field Solvers Extract Both Capacitance and Resistance
- Finite Difference and Finite Element Methods are:
  - Optimal for Complex and Curved 3D Shapes
- Boundary Element and Random Walk Methods are:
  - Optimal for Squared Off Simple “Manhattan” Shapes
- Simulation Speed versus Shape Complexity Trade-off
- Silvaco uses Field Solvers from Both Category Types

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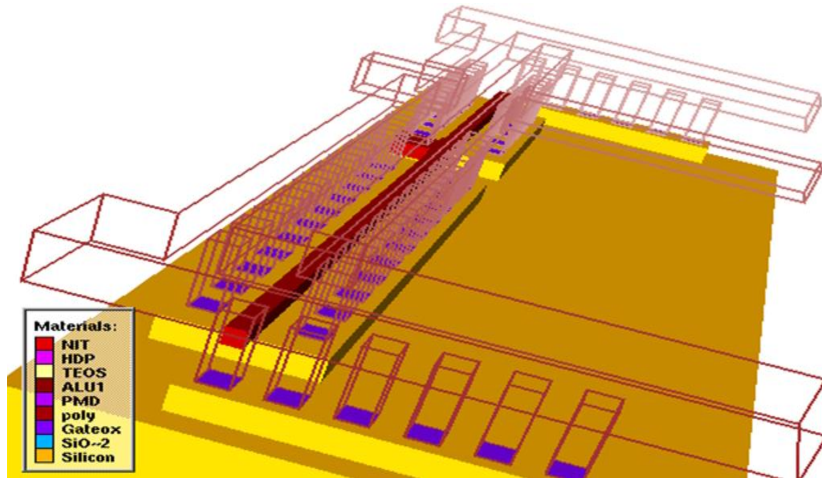
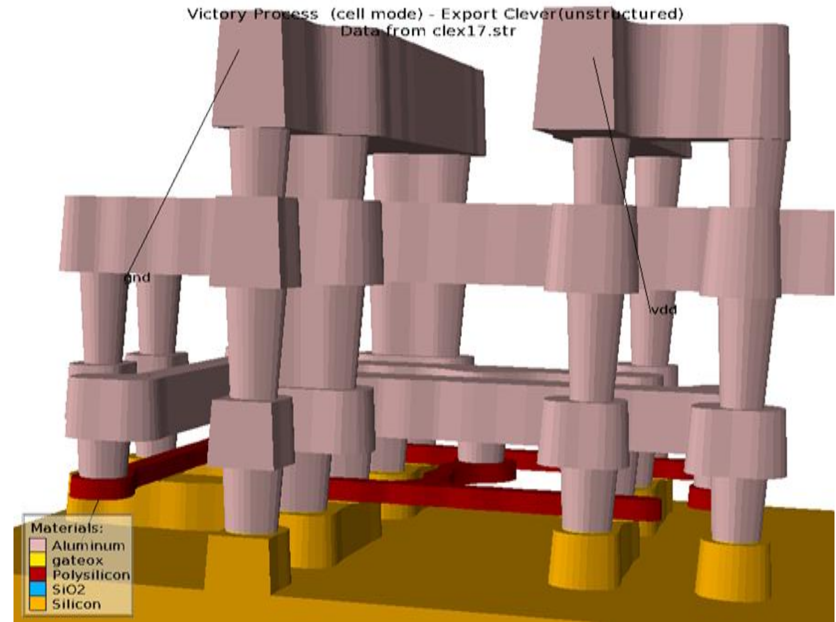
Boundary Element or Finite Element ?

- For Uniform Layer Thickness and Manhattan Shapes
  - Boundary Element Method



- For Complex 3D Shapes
  - Finite Element Method



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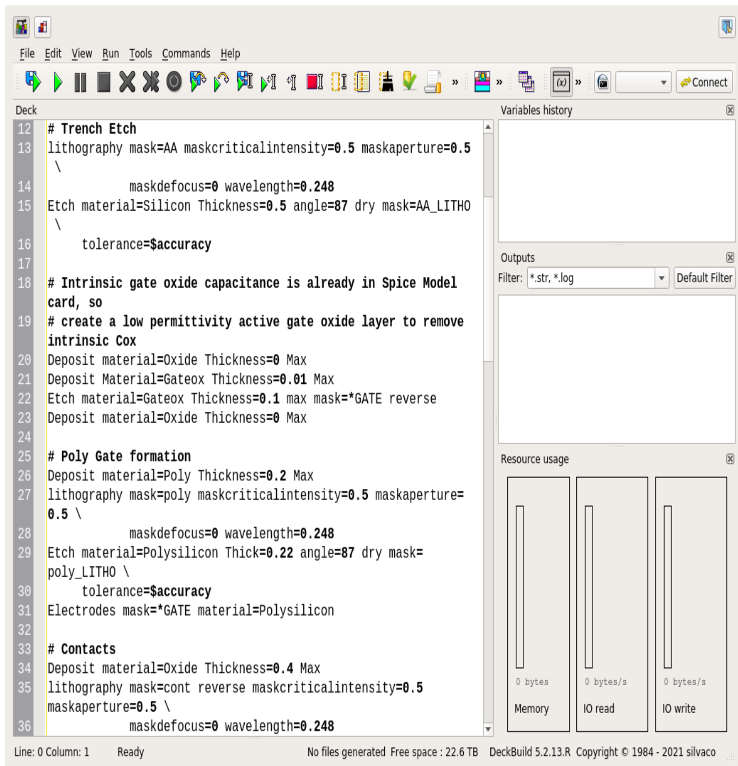
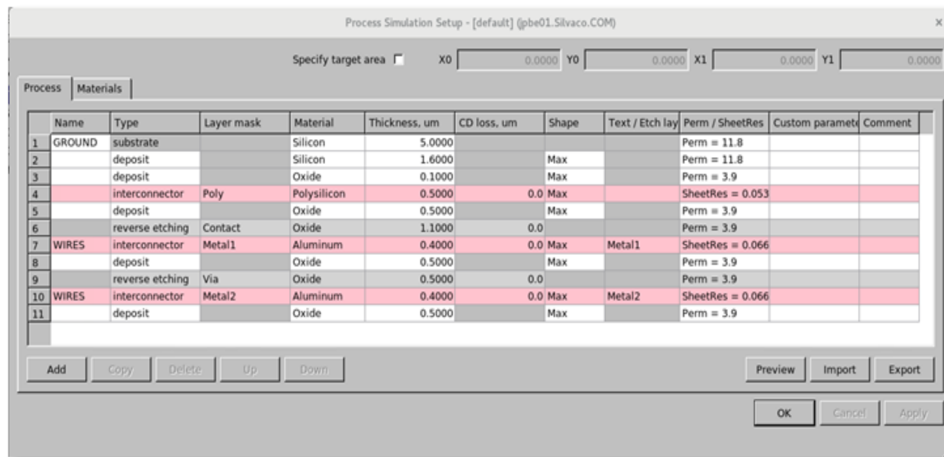
Combining Both Rule and Field Solver Methods



- Technology information for field solved sections can be defined in several ways:
  - 1/ Using TCAD tools and syntax (Left)
  - 2/ Using a GUI in the Layout Tool (Below)
  - 3/ A file provided from the PDK
- Choices for TCAD or CAD Engineers



Process Simulation Setup - [default] (pbe01.Silvaco.COM)

Specify target area X0 0.0000 Y0 0.0000 X1 0.0000 Y1 0.0000

Process | Materials

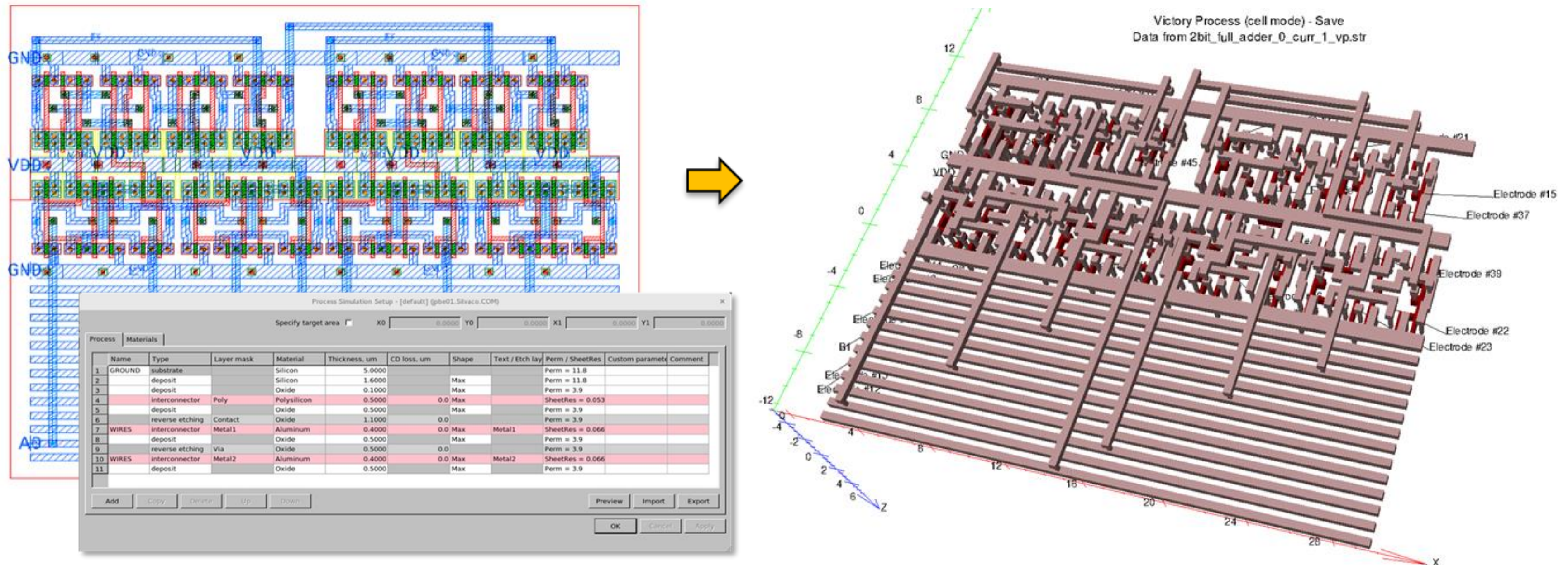
	Name	Type	Layer mask	Material	Thickness, um	CD loss, um	Shape	Text / Etch lay	Perm / SheetRes	Custom paramete	Comment
1	GROUND	substrate		Silicon	5.0000				Perm = 11.8		
2		deposit		Silicon	1.6000		Max		Perm = 11.8		
3		deposit		Oxide	0.1000		Max		Perm = 3.9		
4		interconnector	Poly	Polysilicon	0.5000	0.0	Max		SheetRes = 0.053		
5		deposit		Oxide	0.5000		Max		Perm = 3.9		
6		reverse etching	Contact	Oxide	1.1000	0.0			Perm = 3.9		
7	WIRES	interconnector	Metal1	Aluminum	0.4000	0.0	Max	Metal1	SheetRes = 0.066		
8		deposit		Oxide	0.5000		Max		Perm = 3.9		
9		reverse etching	Via	Oxide	0.5000	0.0			Perm = 3.9		
10	WIRES	interconnector	Metal2	Aluminum	0.4000	0.0	Max	Metal2	SheetRes = 0.066		
11		deposit		Oxide	0.5000		Max		Perm = 3.9		

Add Copy Delete Up Down Preview Import Export

OK Cancel Apply

Combining Both Rule and Field Solver Methods

- Technology information plus layout is converted into a true 3D model of the BEOL for Field Solve



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4		interconnector	Poly	Polysilicon	0.5000	0.0	Max		SheetRes = 0.053		
5		deposit		Oxide	0.5000		Max		Perm = 3.9		
6		reverse etching	Contact	Oxide	1.1000	0.0			Perm = 3.9		
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11		deposit		Oxide	0.5000		Max		Perm = 3.9		

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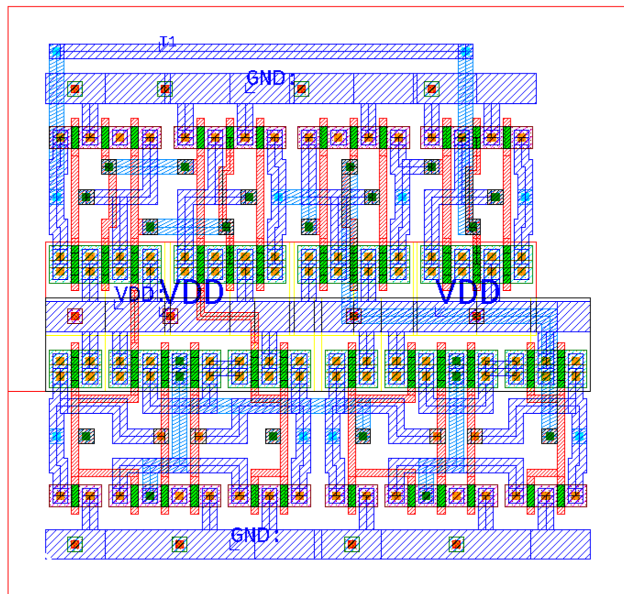
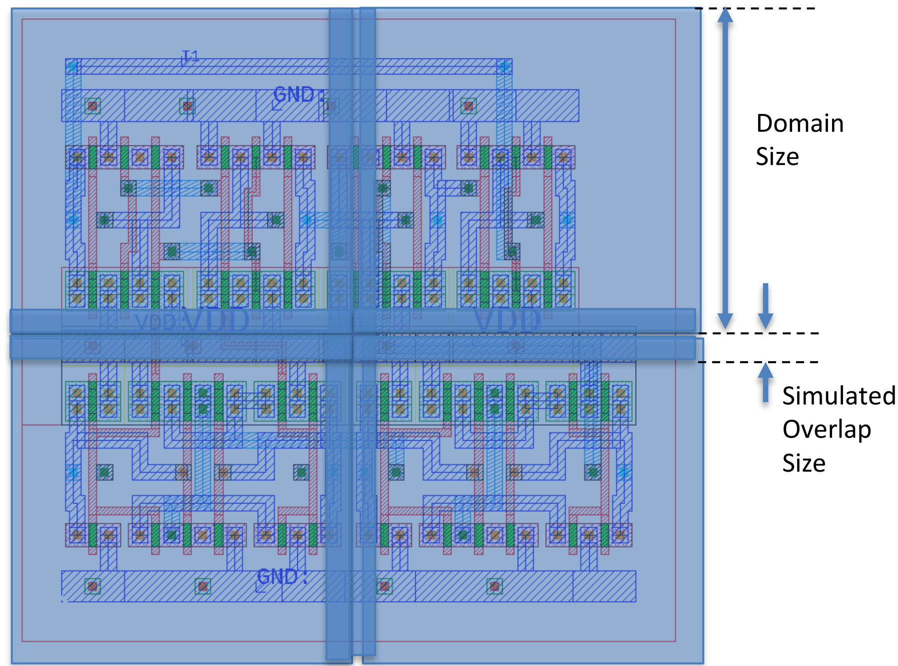
Combining Both Rule and Field Solver Methods

- Domain decomposition allows much larger circuit sections to be field solved





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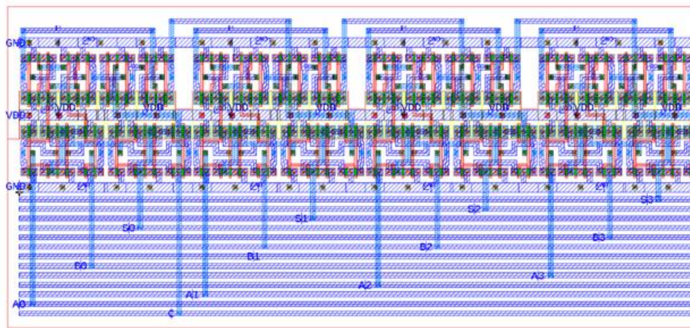
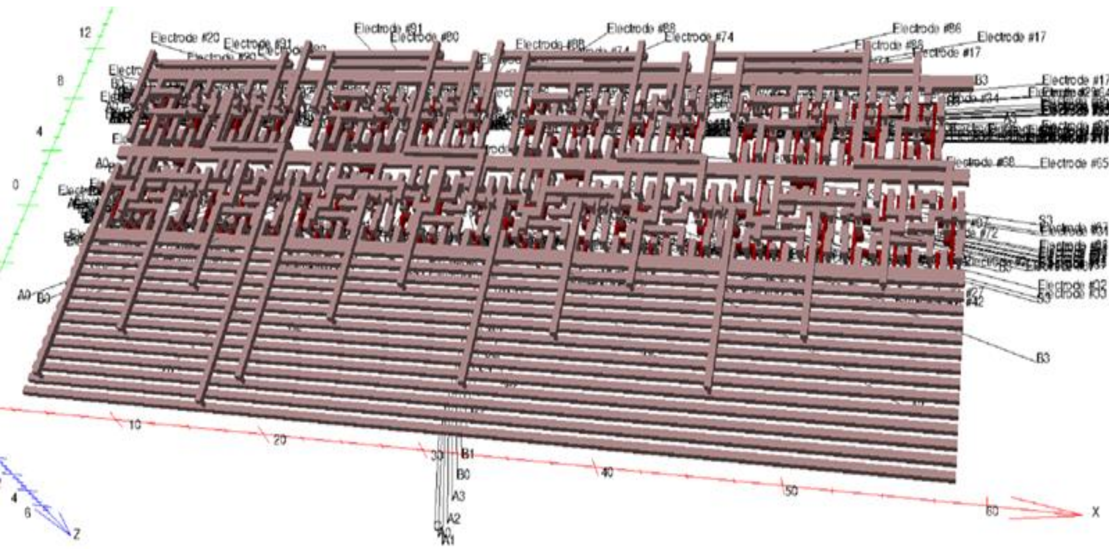
Combining Both Rule and Field Solver Methods

- Simulating a larger overlap improves accuracy a little at the expense of simulation speed.

Example of full 4-bit adder below, using boundary element method, simulation time 26 minutes, 41 seconds using 4 CPUs





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Combining Both Rule and Field Solver Methods

- True Mix and Match Capability in One Tool

User selects which section of the layout is solved using finite element or boundary element field solvers, with the remainder using traditional rule-based extraction

Parasitic Extraction (Capacitance)

Field Solver

Stellar Clever Include dummy nets

Clever version 3.11.26.R Clever processor number: 2 (Max=36)

Include dang nets

Decomposition

Stripes

Stripe width (um) 300

Vicinity width (um) 100

Boxes

Size X (um) 600

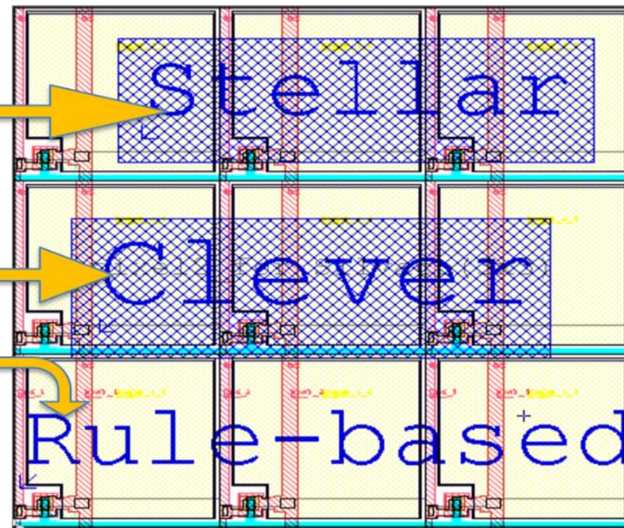
Size Y (um)

Vicinity X (um) 40

Vicinity Y (um) 40

Mix-and-Match (Block dimensions / Solver type and options / Decomposition parameters)

MinX	MinY	MaxX	MaxY	OverlapX	OverlapY	Extraction	Options	SizeX	SizeY	VicinityX	VicinityY
100.000	420.000	566.000	566.000	40.000	20.000	Stellar	...	233.000	146.000	30.00	20.000
52.000	196.000	530.000	360.000	45.000	30.000	Clever	...	240.000	82.000	40.00	25.000



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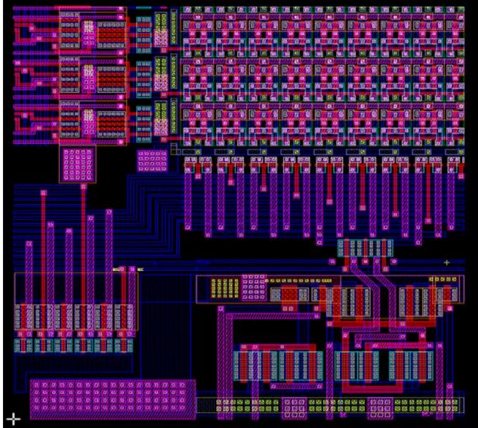
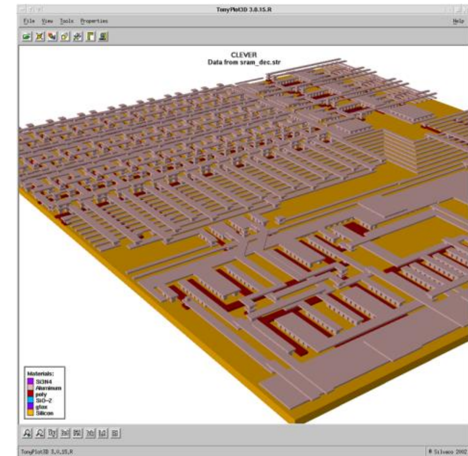
Summary

- Rule Based Extraction – Use for Most of the Full Chip
- Field Solver Extraction – Complex R and C Topology
  - Where Highest Accuracy is Required for Critical Cells
- Mix and Match Techniques within One Design



- Typical Maximum Cell Size illustration for using Field Solve Techniques



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