Top 10 New Features in the SmartSpice 2021 Baseline Release

Introduction

Silvaco's SmartSpice™ is a high-performance parallel SPICE simulator which provides a proven and comprehensive analysis solution. Applications range from complex, high-precision analog and mixed-signal circuits to flat panel displays and TFT arrays, image sensors, memory designs, custom digital circuits, and characterization of standard cell libraries of advanced semiconductor processes, among many others.

SmartSpice offers multiple simulation flavors:

- **SmartSpice HPP:** Silvaco's High-Performance Parallel engine, for Fast Analog (a.k.a. Quasi-SPICE) engine;
- **SmartSpice Pro:** Silvaco's FastSPICE engine;
- **SmartSpice RF:** Silvaco's bundled solution with several specialized engines needed for RF analyses;
- **SmartSpice Server:** Silvaco's solution for distributed simulation across nodes in a network;
- **Harmony:** For general analog/digital co-simulation;

and many more, as listed on www.silvaco.com/.

Silvaco's SmartSpice team around the world has been working constantly to improve the tool's quality and address customer requests. The team strives to make SmartSpice an industry-leader SPICE simulator, and they have been successful in achieving a significant measure towards this goal over the last year.

In this document, we describe the top 10 new features and improvements enabled by the SmartSpice team during this last year. In this case, we are comparing the 2021 Baseline Release, SmartSpice 5.0.3.R, against the 2020 Baseline Release, SmartSpice 4.44.3.R.

The Top 10 new features and improvements are focused on the following aspects:

1. **Performance and capacity improvements:** Up to 4x speedup and 9x memory reduction;
2. **Support for RHELS/CentOS 8:** A key enabler for those migrating away from RHEL/CentOS 6;
3. **New Graphical User Interface (GUI) technology:** Faster and more stable experience;
4. **Improvements on SmartSpice RF:** Completely revised periodic steady-state and phase noise flows;
5. **Improvements on SmartSpice Pro:** A variety of enhancements for a better user experience;
6. **Improved Spectre® compatibility mode:** Key enablers for simulations using the Spectre language;
7. **Improvements on SmartSpice Server:** Cross-platform simulation is now available;
8. **Improved Back Annotation flow:** Extended support to improve robustness;
9. **Improved Parallel `.ALTER` flow:** Control the number of threads of child processes; and
10. **New External Sampling feature:** Set yourself the values for statistical parameters when running Monte Carlo simulations.

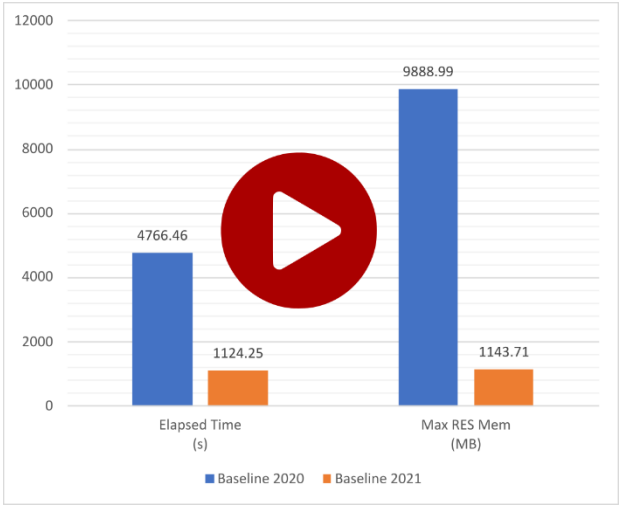
Continue reading and watch the embedded videos to learn more about each of these features.

1. Performance and Capacity Improvements

Performance (the ability to complete simulations in a shorter turnaround time without losing accuracy) and capacity (the ability to simulate larger circuits) has always been two of the main R&D focuses of any SPICE simulator. This is certainly not different for the SmartSpice products.

Over the last year, great improvements have been made within this regard, and the SmartSpice team is happy to announce that SmartSpice 5.0.3.R (Baseline 2021) is much faster and memory optimized when compared to SmartSpice 4.44.3.R (Baseline 2020) for off-the-shelf simulations. In some cases, one can see modest 1.10x speedup and/or 1.03x memory reduction. In other cases, the improvements can be more significant, with around 2x speedup and 2x memory reduction, simultaneously. In a few other cases, the gains are even higher, going around 4-5x speedup and around 9-10x memory reduction, simultaneously.

The following video presents more details about these improvements.



2. Support for RHEL/Centos 8

In terms of Operating System (OS) and Platform support, the Silvaco tools released with Baseline 2020, last Summer, supported 64-bit platforms based on the following operating systems:

- Red Hat Enterprise Linux (RHEL) 6 and 7;
- CentOS Linux 6 and 7; and
- Windows Professional 7, 8, 8.1 and 10.

Focusing on the UNIX-based OS, Maintenance Support for RHEL/CentOS 6 ended on November 30, 2020. With that, many users are considering migrating to RHEL 8, or other EL-based OS. In order to enable them for such a migration, the SmartSpice team is happy to announce that the SmartSpice products now support RHEL/CentOS 8 as well. This includes all SmartSpice products, including Harmony.

An important comment, though, is that the CentOS Linux distributions have been historically released as rebuilds of RHEL distributions. However, this is changing this year. CentOS Linux 8, as a rebuild of RHEL 8, will end on Q4 2021. CentOS Stream continues after that date, serving as the upstream (development) branch of RHEL.

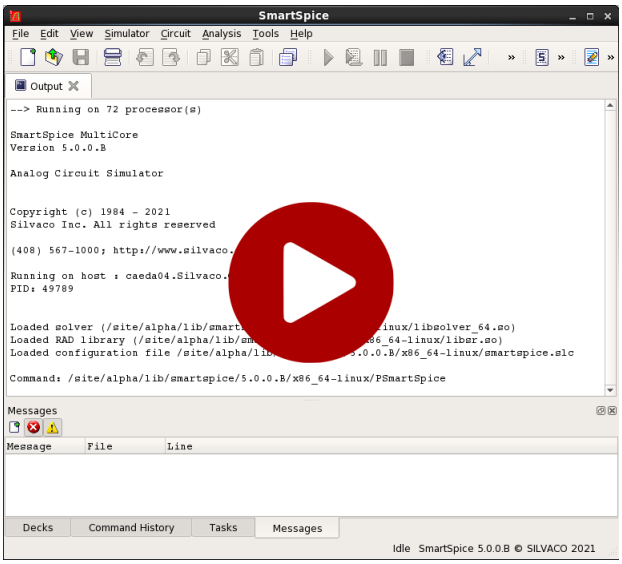
There is still some uncertainty about which new Linux distribution will take place as a rebuild of RHEL. Nonetheless, one should rest assured that, whenever more clarity is brought to this context, the SmartSpice and the Silvaco teams will work diligently to stay up to date with it.

3. New GUI Technology

Another major change in SmartSpice for this 2021 Baseline release is the technology underlying its graphical user interface (GUI). Yet, it is worth mentioning that very minimal differences are noticeable from a user experience perspective right now. The main focus of this enhancement is on the graphic engine itself. This is the first of a crucial two-step process towards an improved interface, planned to be finished by Baseline 2022.

The new GUI, which has just been released, not only brings to SmartSpice the state of the art in terms of graphics and window rendering, but it is also an enabler. Its new technology improves performance and robustness, also allowing for new degrees of testability and maintainability. This all reflects on a faster and more stable experience.

As it is based on a brand-new engine, some of the GUI preferences are not automatically inherited from previous versions. In this case, the users are strongly recommended to run SmartSpice with the “-qt3” flag (which will bring the old engine up), export the preferences, run SmartSpice again (now with the new GUI), and import the preferences back in. The following video quickly introduces the new GUI and demonstrates this export/import process.

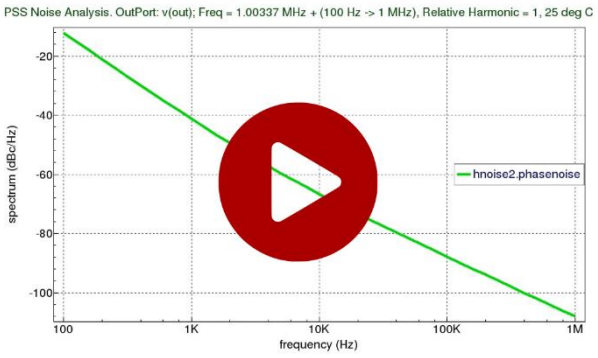


4. Improvements on SmartSpice RF

The 2021 Baseline release also brings a collection of exciting enhancements for SmartSpice RF. Most of these improvements are related to a completely revisited Shooting-Newton-based phase noise analysis flow. Major changes were made:

1. A much improved ***.pss*** analysis, with a more robust periodic steady-state algorithm including better support for oscillator circuits; as well as
2. A brand new Perturbation Projection Vector (PPV) algorithm for more accurate oscillator phase noise analysis.

The following video introduces these improvements and demonstrates its benefits on a circuit.



The simulation setup demonstrated in this video is shipped along with the 2021 Baseline release. Please, feel free to try it yourself.

Much more is still to come. For the 2022 Baseline, the SmartSpice team plans to release an enhanced ***pnoise***/***hnoise*** analysis, now with a Frequency-Aware PPV capability. This will allow SmartSpice RF to capture long time-constant effects. The team is also planning to start revisiting our Harmonic Balance flow. So, please, stay tuned!

5. Improvements on SmartSpice Pro

With the ever-growing complexity of circuit designs, the challenges of verification are intensified. In some of the cases, regular SPICE simulation cannot deliver the desired set of results in due time, and FastSPICE engines become necessary. This is when SmartSpice Pro comes into play.

Over the last year, SmartSpice Pro has also received good attention from our R&D team. With this, a variety of improvements are being made available on its 2021 Baseline release, such as:

- Improved flows for bisection optimizations and Monte Carlo analyses;
- Improved partitioning algorithms;
- Improved support for PWL voltage and current sources;

along with many other fixes.

We strongly encourage you to download the tool and check it out by yourself.

6. Improved Spectre Compatibility Mode

SmartSpice is not only a proven, mature SPICE simulator. It is also one of the most flexible simulators in the market. We count first on our 30+ years of feature, model and analysis development, which bring to our users a variety of unique features. On top of that, we have a strong HSPICE® compatibility mode, along with an ever-growing Spectre® compatibility mode.

In the 2021 Baseline release, SmartSpice pushed its Spectre support even further, with many improvements that are key enablers for the simulation of circuits using Spectre language, or even SPICE-described circuits relying on Spectre models. A few of these improvements are listed below:

- Improved support for the TSMC Model Interface (TMI) under Spectre mode;
- Improved handling of user-defined functions and parameters in Spectre mode;
- Added support for new models; and
- Improved support for general Spectre syntax;

among many others.

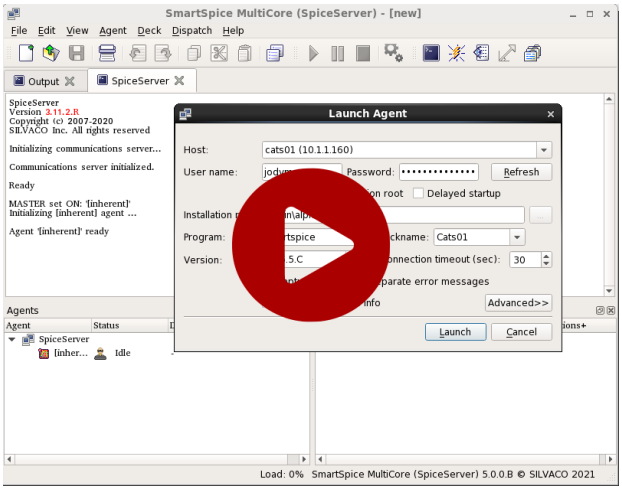
It would be a pleasure to have you trying SmartSpice's Spectre compatibility mode.

7. Improvements on SmartSpice Server

SmartSpice Server brings the capability of running distributed jobs. With this, SmartSpice users are able to execute a server process on a given node on a network and dispatch simulation jobs to multiple other computer nodes in their network or computer farm. Additionally, its unique split and slice functionalities make it possible to take a single, time-consuming job and speed up its simulation time by dividing the simulation in smaller parts and distributing these tasks across nodes in a network. A given customer already reported more than 6x speedup, reducing a 22-hour simulation down to 3.5 hours, just for using this feature.

Up to the 2020 Baseline release, last year, SmartSpice Server was basically working only if servers and agents were based on the same operating system. Now, on the 2021 Baseline release, SmartSpice Server is able to launch jobs in a cross-platform environment, i.e., users can not only dispatch simulations from Linux to Linux or from Windows to Windows (as they could already do before), but they can now also run SmartSpice Server from Linux to Windows or from Windows to Linux as well.

More details about it are presented in the following video:



8. Improved Back Annotation Flow

As technology advances, the need for post-layout simulation becomes more and more real. The effects from parasitic devices are continuously more important, and pre-layout simulation (with an ideal, no-parasitic netlist) tends not to reflect real silicon behavior. With this, running SPICE simulation including layout parasitics is becoming a rule.

Traditionally, the way to handle post-layout simulation is by including the parasitic netlist as a replacement of the pre-layout block. However, as parasitic netlists are usually flat, the advantages of hierarchical-based designing are lost.

Since the 2020 Baseline release, last year, SmartSpice has been supporting another, more optimized flow for this problem, called Post-Layout Back Annotation. With this, SmartSpice is able to read both netlists, take parasitic devices from the DSPF netlist, and annotate them back onto the ideal netlist. This brings to circuit designers the ability to play with the advantages of hierarchical designs and post-layout simulations, simultaneously.

Another major improvement on the 2021 Baseline release is an enhanced Back Annotation flow. A few of the enhancements are listed below:

- Added support for macro models on parasitic netlists; and
- Added support for multiply factors on ideal netlists,

among others.

It is worth mentioning that these enhancements are also supported by the Selective-Net Back Annotation flow.

Please, try the Back Annotation flow included in the 2021 Baseline release. Any related feedback would be most welcome!

9. Improved Parallel .ALTER Flow

The SmartSpice Parallel .ALTER flow is a well-known functionality, much used by customers. In a nutshell, if (a) the input deck contains multiple .ALTER statements, and (b) SmartSpice MultiCore is used, then SmartSpice by default creates a pool of child processes based both on the number of .ALTER statements and the adopted number of cores in the simulation. Then, it will run each .ALTER simulation in parallel, as if they were independent circuits. This is a very interesting feature to speed up the simulation time by taking advantage of the modern multicore hardware platforms.

Until now, each of these child processes was running in a single thread, and the users did not have a way to control the number of threads per child process.

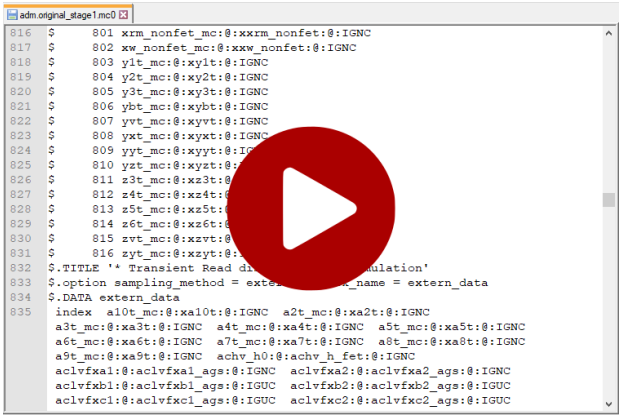
This has changed in the 2021 Baseline release. From this version on, one can now use an extra command-line argument “-PA <numthreads>” and set the number of threads for child process in the parallel .ALTER mode.

It is strongly recommended to download the tool and check it out on your own.

10. New External Sampling Feature for Monte Carlo Analyses

When running a Monte Carlo analysis, the default behavior of a SPICE simulator is to adopt one of its built-in sampling algorithms and, for each Monte Carlo iteration, set random values for each of the statistical parameters in the circuit, according to their associated distribution. Although it is not generally a problem, this methodology makes it difficult for design and process exploration when it comes to statistical experiments.

In the 2021 Baseline, SmartSpice presents its first release of External Sampling. This new functionality allows our users to set the values for statistical parameters themselves when running Monte Carlo simulations. The following video demonstrates the process in more details.



As this is only its first release, more is still to come. The upcoming Quarterly Releases should extend the functionality, e.g. adding support for TMI models. If this topic is of any interest, please, stay tuned!