Hipex RC: 7 Techniques for Reducing a RC Netlist

Introduction

Hipex RC is accurate and fast full-chip hierarchical extraction software that performs extraction of parasitic capacitances and resistances from hierarchical layouts. Parasitic RC netlists are sometimes too large to run post-layout simulation. Hipex RC provides several methods to reduce large RC netlists, and this application note introduces seven techniques for doing so.

1. Merge series resistances

Select “Parasitic Extraction” in “Layout Parameter Extraction Setup” window, and enter “Serial merge threshold (Ohm)” value of “Resistance Extraction” (Figure 1). A resistance, which is below a given threshold, merges with the biggest resistance next to it (Figure 2).

This is effective for eliminating the many small resistances that can be generated in long distance interconnects with many corners.

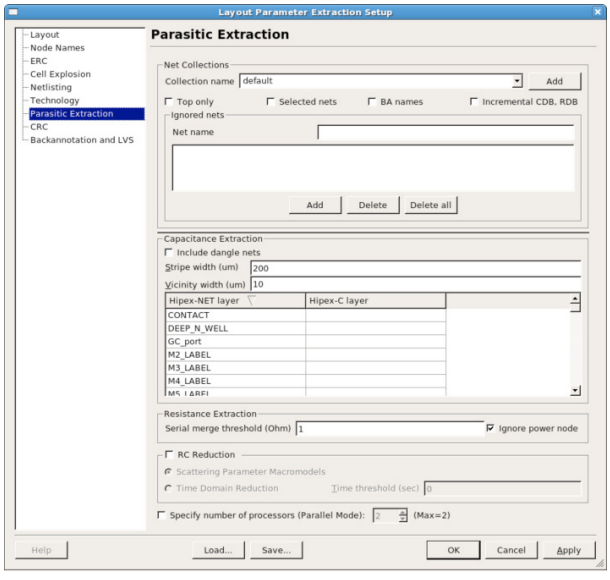

Figure 1. Serial merge threshold setup.

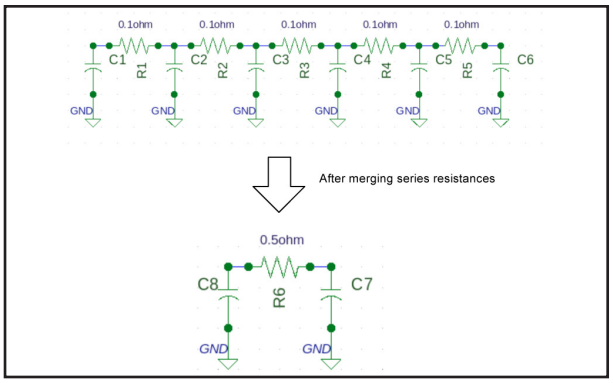

Figure 2. Effect of merging resistances by 1ohm.

2. Merge coupling capacitances into ground capacitances

Select “Netlisting” in “Layout Parameter Extraction Setup window”, and enter “Coupling threshold” value of “Parasitic capacitor netlist” (Figure 3).

Hipex RC does not report coupling capacitances below this threshold. Instead, it contributes them to the ground capacitances of the two coupling (Figure 4).

This is effective if small coupling capacitances can be ignored.

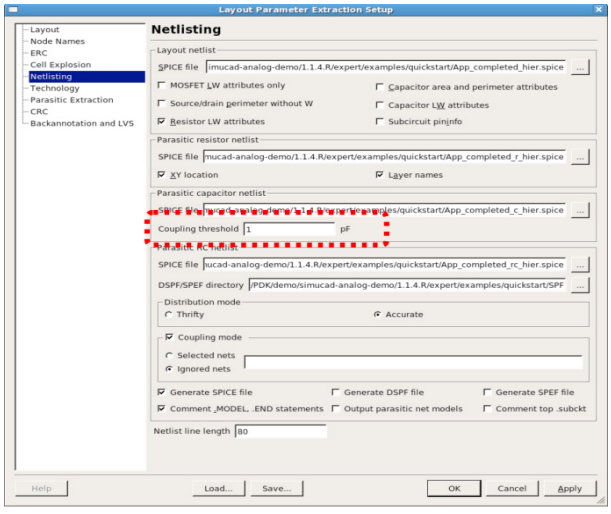

Figure 3. Coupling threshold setup.

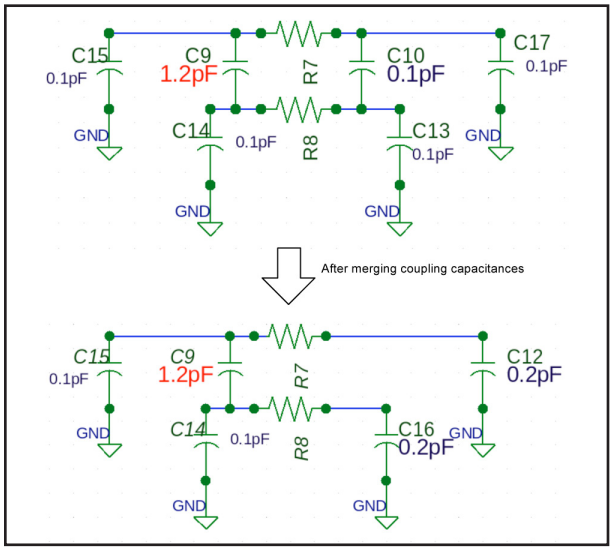

Figure 4. Effect of merging capacitances by 1pF.

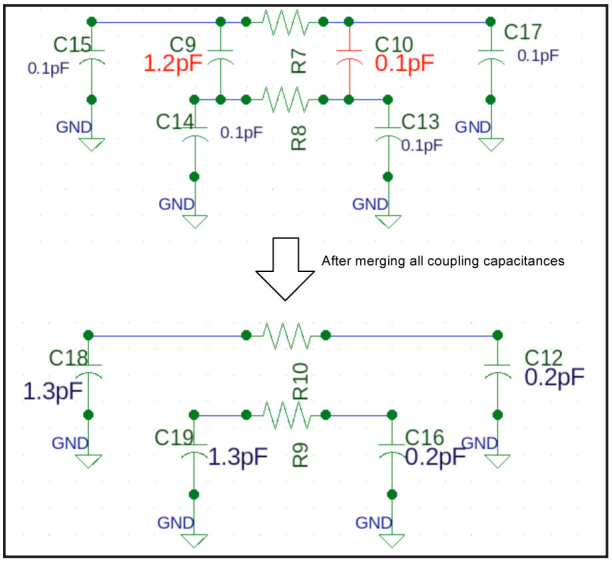

Figure 6. Effect of disabling coupling capacitances.

3. Disable coupling capacitances mode

Select “Netlisting” in “Layout Parameter Extraction Setup window”, and disable “Coupling mode” of “Parasitic RC netlist” (Figure 5).

Hipex RC does not report all coupling capacitances. Instead, it contributes them to the ground capacitances.

This is effective if the effect of all coupling capacitances can be ignored.

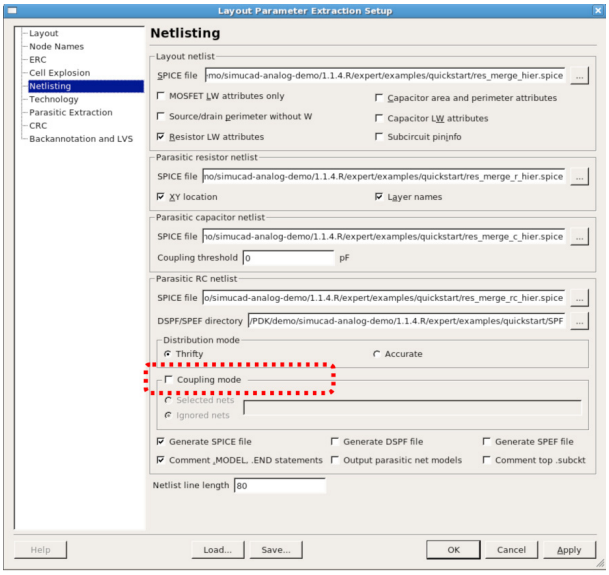

Figure 5. Disable coupling mode.

4. Selective cells and nets

Hipex RC can extract only selected cells and nets. This method is described in detail in another application note, “Selective RC-extraction Methods in Guardian LPE for Post-layout Circuit Simulations”.

This is effective if you know in advance which cells and nets are critical for the circuit.

5. Thrifty mode

Select “Netlisting” in “Layout Parameter Extraction Setup window”, and select “Thrifty” under “Distribution mode” (Figure 7).

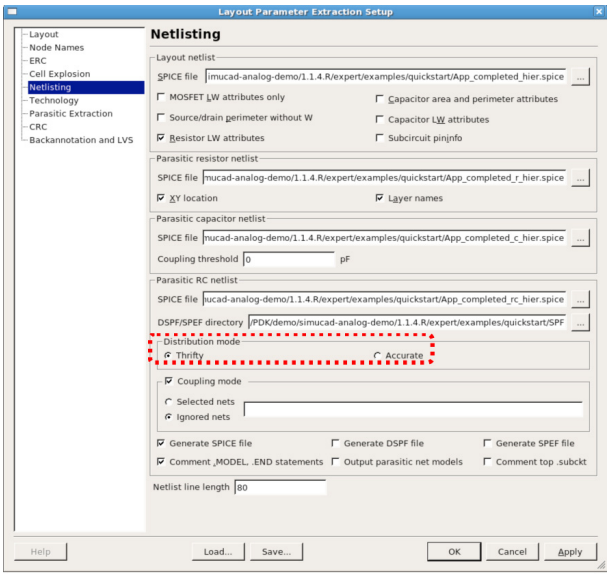

Figure 7. Select Thrifty mode.

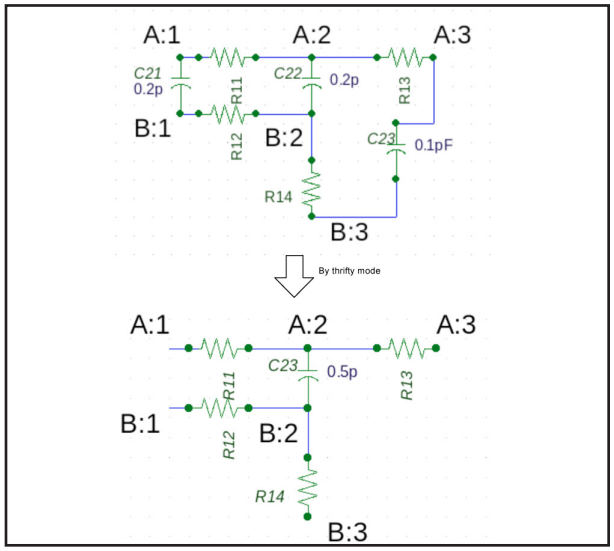

Figure 8. Effect of thrifty mode.

In thrifty mode, Hipex RC extracts only a capacitance per couple of nodes. As shown in Figure 8, there are three capacitances between “A” node and “B” node. These capacitances are reduced to one capacitance by thrifty mode.

This is effective if accuracy of relative positions for interconnects is not necessary.

6. Built-in RC Reduction

Select “Parasitic Extraction” in the “Layout Parameter Extraction Setup window”, and enable “RC Reduction” (Figure 9). Hipex RC uses two techniques for the built-in RC reduction. The first one is based on the Scattering Parameter Macromodeling method. The second one is based on the time constant reduction method.

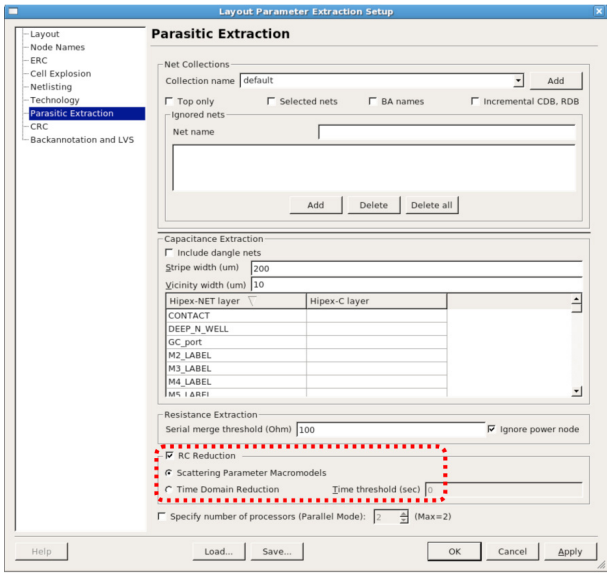

Figure 9. RC Reduction setup.

Both methods eliminate a node in a parasitic net with a small RC value by distributing this value to neighborhood nodes.

For more detailed information refer to section 4.5 ”RC Reduction in HipexNetlister” in the Hipex User’s Manual.

7. RC Reduction using ClarityRLC

Select “CRC” in “Layout Parameter Extraction Setup window”, and set up the options in this window (Figure 10).

Using this reduction method, ClarityRLC is executed from Expert’s menu after Hipex RC execution. ClarityRLC is a powerful reduction tool and has several options for reducing RLC netlists.

For more detailed information refer to the ClarityRLC User’s Manual.

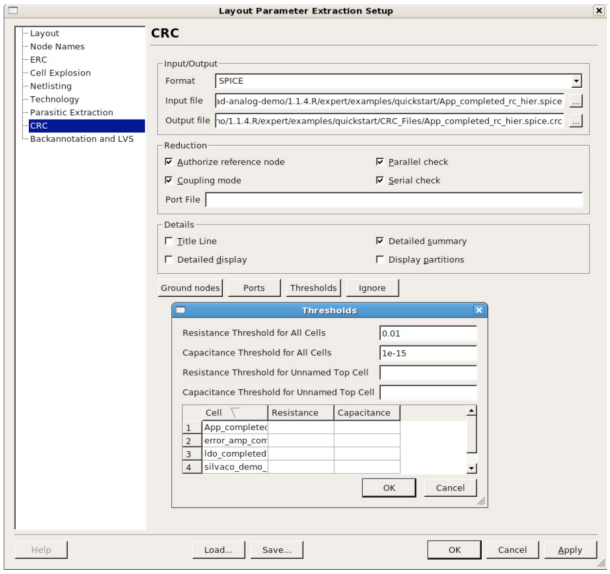

Figure 10. ClarityRLC setup.

Conclusion

Hipex RC has enough options to reduce RC netlists. Users can select which combinations are best according to the target circuits. ClarityRLC can efficiently and accurately reduce linear parasitic RLC elements in parasitic extracted netlist. Using these techniques, users can reduce parasitic capacitances and resistances thus significantly reducing runtime of post-layout simulations.