Parasitic Back Annotation for Post Layout Simulation

Introduction:

Layout designers have different layout approaches to try to minimize the parasitic effects created by the physical layout. However, post layout simulation is often required to ensure proper functionality of the design and to better represent the final silicon product behavior. This application note will describe the different steps required to back annotate the parasitic effects to your netlist in order to perform post layout simulation

The Extraction and LVS step:

In this application note it is assumed that the user already has a clean LVS between the layout extracted netlist and the schematic netlist. If this is not the case, the user can get some guidance on how to achieve clean LVS by referring to the application note titled “A Suggested Approach for Layout Versus Schematic (LVS) comparison using Guardian LVS”, found on the Silvaco website at the following link: (https://silvaco.com/wp-content/uploads//content/appNotes/iccad/2-004_LVSComparision.pdf).

At the completion of the LVS clean step, the user needs to save two files that will be needed in the back annotation process. The first file is the schematic netlist used in the LVS run and the second file is the LVS setting criteria, which can be saved in the Guardian LVS tool, under Setup>>Project Setting>> with the use of the save button located in the lower left corner. This setup will be saved as a *.gpr file. Figure 1 illustrates the Project setting window with the save option.

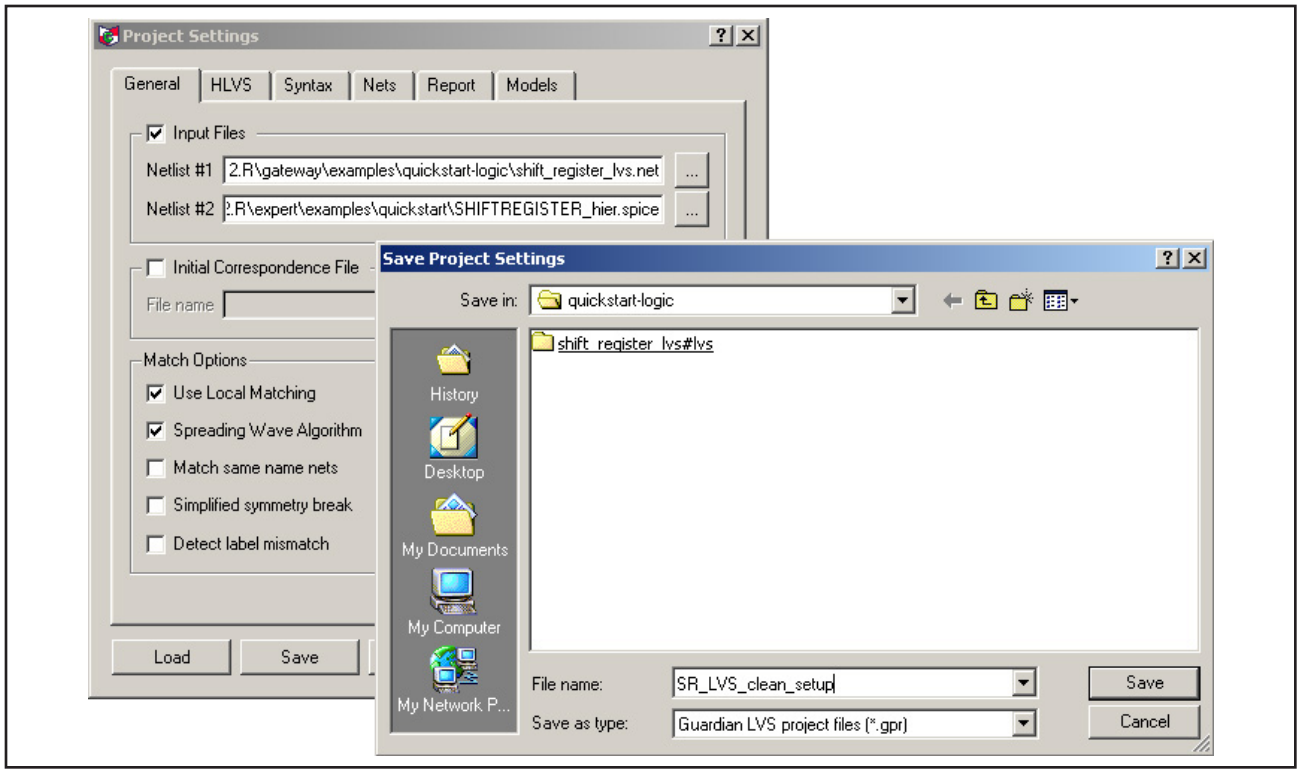

Figure 1: Saving LVS setting to *.gpr file.

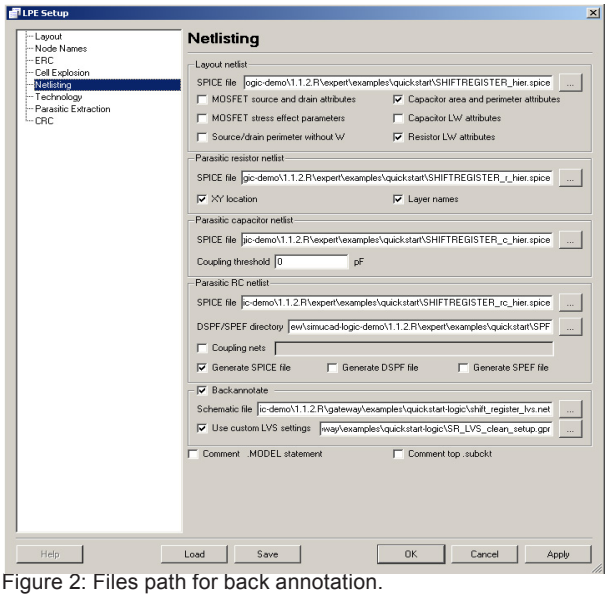

Figure 2: Files path for back annotation.

The *.gpr file will be useful because this is how the tool can establish a correspondence between the schematic netlist (front end netlist) and the ayout extracted netlist (back end netlist). The Match report of the Guardian LVS tool will be used to correlate the back end net name with the equivalent front end net name.

```
**************************************************
* Sub-Circuit Netlist of : nand2
**************************************************
.subckt nand2 #2 #3 #4 #5 #6
M#2 #1 #6 #4 #4 CMOSN  L=2U W=5U
M#3 #3 #5 #2 #3 CMOSP  L=2U W=10U
M#4 #2 #6 #3 #3 CMOSP  L=2U W=10U
M#1 #2 #5 #1 #4 CMOSN  L=2U W=5U
.ends nand2

**************************************************
* Sub-Circuit Netlist of : NAND_3
**************************************************
.subckt NAND_3 #10 #11 #12 #13 #14 #7
M#8 #7 #12 #10 #7 CMOSP  L=2U W=10U
M#9 #10 #13 #7 #7 CMOSP  L=2U W=10U
M#10 #7 #14 #10 #7 CMOSP  L=2U W=10U
M#6 #8 #13 #9 #11 CMOSN  L=2U W=5U
M#7 #9 #14 #10 #11 CMOSN  L=2U W=5U
M#5 #11 #12 #8 #11 CMOSN  L=2U W=5U
.ends NAND_3

**************************************************
* Sub-Circuit Netlist of : D_FF
**************************************************
.subckt D_FF #15 #16 #21 #22 #23 #24
XI5 #17 #21 #19 #24 #20 #15 NAND_3
XI0 #22 #15 #21 #20 #23 nand2
XI1 #18 #15 #21 #19 #20 nand2
XI2 #23 #15 #21 #22 #17 nand2
XI3 #19 #15 #21 #17 #16 nand2
XI4 #20 #15 #21 #18 #24 nand2
.ends D_FF

**************************************************
* Sub-Circuit Netlist of : SHIFTREGISTER
**************************************************
.subckt SHIFTREGISTER
XI0 #36 #28 #29 #27 #26 #34 D_FF
XI1 #36 #31 #29 #28 #30 #34 D_FF
XI2 #36 #33 #29 #31 #32 #34 D_FF
XI3 #36 #25 #29 #33 #35 #34 D_FF
.ends SHIFTREGISTER
.end
```

Figure 3: Layout Netlist.

The first step in the back annotation process is to back annotate the schematic netlist net name to the layout extracted netlist. This is an important step, as the schematic net names are the ones used in the imulation. They are the nets to which the stimuli are passed in the-circuit simulation. In order to back annotate the nets to the schematic netlist, the user needs to perform a simple layout netlist extraction, without the parasitics, but this time the user needs to specify to back annotate to the schematic netlist. In the LPE Setup of Expert, the user needs to choose the “Netlisting” tab and select the check box “Backannotate”. This enables the user to specify the path to the Schematic netlist that was used during the LVS match and the path to the LVS setting to achieve

LVS clean. Figure 2, illustrates these steps. In reality, the resultant netlist is still the layout extracted netlist, with the same netlist hierarchy, in which the nets name have been substituted by the equivalent nets name from the schematic netlist.

Figure 3 illustrates the layout extracted netlist of a shift register without back annotation and figure 4 shows the schematic netlist of the same circuit. The resultant netlist, when the back annotation option is selected, is shown in figure 5. As can be observed, the hierarchical structure of the netlist as well as the level of parameter detail is preserved; only the nets name are substituted.

```
X1 C NET7 OUT0 NET1 VDD GND DFF
X2 C OUT0 OUT1 NET3 VDD GND DFF
X3 C OUT1 OUT2 NET5 VDD GND DFF
X4 C OUT2 OUT3 NET4 VDD GND DFF
*
* Schematic name: DFF
*
.SUBCKT DFF C D Q Q_bar VDD VSS
*
X1 NET13 Q_bar Q VDD VSS NAND2
X2 Q NET10 Q_bar VDD VSS NAND2
X3 NET10 D NET8 VDD VSS NAND2
X4 NET12 C NET13 VDD VSS NAND2
X5 NET8 NET13 NET12 VDD VSS NAND2
X10 NET13 C NET8 NET10 VDD VSS NAND3
*
.ENDS DFF
*
* Schematic name: NAND2
*
.SUBCKT NAND2 IN1 IN2 OUT VDD VSS
*
M1 OUT IN1 NET2 VSS CMOSN L=2U W=5U AD=27.5P AS=27
M2 NET2 IN2 VSS VSS CMOSN L=2U W=5U AD=27.5P AS=27
M3 OUT IN1 VDD VDD CMOSP L=2U W=10U AD=55P PD=31U
M4 OUT IN2 VDD VDD CMOSP L=2U W=10U AD=55P PD=31U
*
.ENDS NAND2
*
* Schematic name: NAND3
*
.SUBCKT NAND3 IN1 IN2 IN3 OUT VDD VSS
*
M1 OUT IN1 NET2 VSS CMOSN L=2U W=5U AD=27.5P AS=27
M2 NET2 IN2 NET1 VSS CMOSN L=2U W=5U AD=27.5P AS=2
M3 OUT IN1 VDD VDD CMOSP L=2U W=10U AD=55P PD=31U
M4 OUT IN2 VDD VDD CMOSP L=2U W=10U AD=55P PD=31U
M5 NET1 IN3 VSS VSS CMOSN L=2U W=5U AD=27.5P AS=27
M6 OUT IN3 VDD VDD CMOSP L=2U W=10U AD=55P PD=31U
*
.ENDS NAND3
*
```

Figure 4: Schematic Netlist.

```
*****************************************
* Sub-Circuit Netlist of : NAND2
*****************************************
.subckt NAND2 OUT VDD VSS IN1 IN2
M2 NET2 IN2 VSS VSS CMOSN  L=2U W=5U
M3 VDD IN1 OUT VDD CMOSP  L=2U W=10U
M4 OUT IN2 VDD VDD CMOSP  L=2U W=10U
M1 OUT IN1 NET2 VSS CMOSN  L=2U W=5U
.ends NAND2

*****************************************
* Sub-Circuit Netlist of : NAND3
*****************************************
.subckt NAND3 OUT VSS IN3 IN2 IN1 VDD
M6 VDD IN3 OUT VDD CMOSP  L=2U W=10U
M4 OUT IN2 VDD VDD CMOSP  L=2U W=10U
M3 VDD IN1 OUT VDD CMOSP  L=2U W=10U
M2 NET1 IN2 NET2 VSS CMOSN  L=2U W=5U
M1 NET2 IN1 OUT VSS CMOSN  L=2U W=5U
M5 VSS IN3 NET1 VSS CMOSN  L=2U W=5U
.ends NAND3

*****************************************
* Sub-Circuit Netlist of : DFF
*****************************************
.subckt DFF VDD D VSS Q Q_bar C
X10 NET10 VSS NET8 C NET13 VDD NAND3
X1 Q VDD VSS NET13 Q_bar NAND2
X5 NET12 VDD VSS NET8 NET13 NAND2
X2 Q_bar VDD VSS Q NET10 NAND2
X3 NET8 VDD VSS NET10 D NAND2
X4 NET13 VDD VSS NET12 C NAND2
.ends DFF

*****************************************
* Sub-Circuit Netlist of : top
*****************************************
.subckt top
X4 VDD OUT2 GND OUT3 NET4 C DFF
X3 VDD OUT1 GND OUT2 NET5 C DFF
X2 VDD OUT0 GND OUT1 NET3 C DFF
X1 VDD NET7 GND OUT0 NET1 C DFF
.ends top
```

Figure 5: Layout back annotated Netlist.

R, C and RC Exraction with Back Annotation

The parasitic effect of the layout can be accounted for when running the parasitic extraction for capacitor (HIPEX-C), resistor (HIPEX-R) or a combination of the two using HIPEX-RC. These three modes of parasitic extraction can all be launched from within Expert. The parasitic coefficients for the given process need to be specified through the LPE setup page, under the tab Technology. These coefficients are provided in two different files, one for the capacitors and one for the resistors. The user needs to specify the path to these files as shown in Figure 6.

In order to extract the parasitic effects of your layout, choose Expert>>Verification>>Extraction>>Hipex-C>>Run, Hipex-R>>Run or Hipex-RC>>Run. The first option of the three will produce an extracted netlist with-the parasitic capacitors only. A portion of the resultant netlist is shown in Figure 7. T he second option will pro-

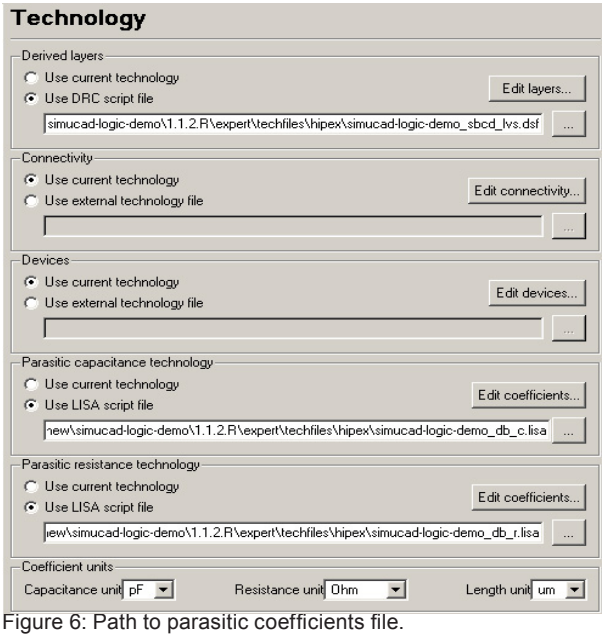

Figure 6: Path to parasitic coefficients file.

```
*****************************************
* Sub-Circuit Netlist of : DFF
*****************************************

.subckt DFF VDD D VSS Q Q_bar C
X10 NET10 VSS NET8 C NET13 VDD NAND3
X1 Q VDD VSS NET13 Q_bar NAND2
X5 NET12 VDD VSS NET8 NET13 NAND2
X2 Q_bar VDD VSS Q NET10 NAND2
X3 NET8 VDD VSS NET10 D NAND2
X4 NET13 VDD VSS NET12 C NAND2

*** Parasitic capacitors ***

Cp1 NET12 NET13 8.31903e-016
Cp2 NET12 NET8 3.88372e-017
Cp3 NET12 SUB 3.82461e-013
Cp4 NET13 NET8 3.88372e-017
Cp5 NET13 SUB 1.14145e-012
Cp6 NET8 NET10 5.32508e-016
Cp7 NET8 SUB 7.69817e-013
Cp8 NET10 SUB 7.60928e-013

.ends DFF
```

Figure 7: Parasitic C back annotated netlist. Figure 9: Parasitic Extraction setup.

duce a netlist with only the parasitic resistors effect, and the Hipex-RC option will generate a netlist as shown in Figure 8, which contains the R and C effect.

As can be seen in Figure 8, a given net can be separated into subnets to allow for the parasitic resistance to be inserted in the circuit. For example, NET12 is now represented by NET12:17 and NET12:25. It can also be noted that the net VDD is broken into many subnets. The LPE Setup page gives the user some flexibility on how the parasitic components need to be extracted. These options are described in the following section.

```
*
* Sub-Circuit Netlist of : DFF
*
********************************************************************************

.subckt DFF VDD:219 VDD:144 VDD:143 VDD:157 VDD:151 VDD:153 VDD:154 VDD:155
+VDD:149 VDD:140 VDD:142 VDD:141 VDD:148 VDD:147 D:40 D:39 VSS Q:36 Q:41 Q:42
+Q_bar:23 Q_bar:22 Q_bar:18 C:138 C:140 C:139 C:137
X10 NET10:31 VSS NET8:39 NET8:38 C:138 C:140 NET13:45 NET13:44 VDD:219 VDD:144
+VDD:143 VDD:157 NAND3
X1 Q:36 VDD:219 VDD:151 VDD:153 VSS NET13:47 NET13:46 Q_bar:23 Q_bar:22 NAND2
X5 NET12:19 VDD:219 VDD:154 VDD:155 VSS NET8:41 NET8:40 NET13:48 NET13:49 NAND2
X2 Q_bar:18 VDD:219 VDD:149 VDD:140 VSS Q:41 Q:42 NET10:34 NET10:35 NAND2
X3 NET8:33 VDD:219 VDD:142 VDD:141 VSS NET10:37 NET10:36 D:40 D:39 NAND2
X4 NET13:39 VDD:219 VDD:148 VDD:147 VSS NET12:22 NET12:21 C:139 C:137 NAND2

*** Parasitic resistors ***

Rp1 NET12:17 NET12:25 0.034358
* Layer METAL2 at (19.5, 31.5)
Rp2 NET12:17 NET12:29 56.910566
* Layer connect_poly at (19.5, 31.5)
Rp3 NET12:17 NET12:30 56.910566
* Layer connect_poly at (19.5, 31.5)
Rp4 NET12:29 NET12:30 140.105155
```

Figure 8: Parasitic RC back annotated netlist.

Parasitic Extraction Options:

Under the tab “Netlisting” of the LPE Setup, (see Figure 2) in the section “Parasitic resistor netlist”, the users can specify the path and name of the parasitic resistor netlist. The status of the two check boxes located below the path field will determine if the netlist contains the XY coordinates of the parasitic resistor component and the physical layer leading to this resistance value. In the same page, under the “Parasitic capacitor netlist” section, the parasitic capacitor netlist path and name can be entered.

In addition, the user can specify a coupling threshold.

If the coupling threshold is set to zero, every net can have a parasitic capacitance to every other net. By setting a coupling threshold, the tool will express net to net capacitance only if the capacitance value is above the threshold. All of the capacitance values that are lower than the threshold will be replaced with ground capacitance of the same value. When replacing the coupling capacitance between two nets a corresponding ground capacitance is added to both nets involved.

The RC parasitic section follows, allowing the user to input the path to the netlist and the output format desired (spice, dspf, spef). A check box also allows the user to specify a list of coupling nets. If a list of nets is provided, the extraction tool will consider these nets as the coupling ones. This means that the capacitance for the nets listed will not be grounded.

The tab “Parasitic Extraction” of the LPE Setup window shown in figure 9 offers other setup options to the user.

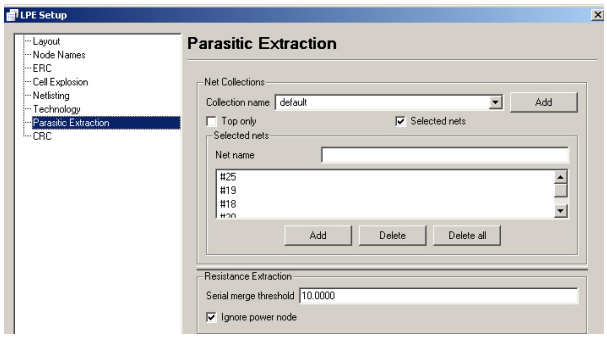

Figure 9: Parasitic Extraction setup.

The parasitic extraction can be performed on a specified list of nets or the user can select to ignore some nets. A serial merge threshold can also be set for the resistors; this will reduce the number of resistors in the netlist. If the threshold is set to 10 Ohms, the tool will combine in series, when possible, every parasitic resistor with a lower value than the threshold. The extraction setup can be saved to a file. This will generate a *.epo file, which can be reloaded at a later time. More about the features and options described can be found in the Guardian User’s manual.

Conclusion:

This application note has described the necessary steps and tool features that will simplify the back annotation of the parasitic effects to the netlist in order to perform a post layout simulation. This procedure should allow the user to better estimate the silicon behavior based on the physical design and assist the designer in order to do the required modifications to the layout and ensure proper functionality of the design.