Central Hipex Database and Improved Hipex C and Hipex R Technology Files

1. Introduction

Layout parameter extraction (LPE) and parasitic extraction play an important role in post-layout verification process. Verification of a full chip layout is increasingly becoming a problem because sizes of IC layouts continue to grow due to new IC technologies. The complexity of IC design demands that designer should consider the effects caused by parasitic capacitors and resistors. Parasitic devices are responsible for effects such as time delay, voltage drop, and signal integrity violation, which lead to low chip performance. But the key problem in IC design is getting an accurate estimation of parasitic devices.

Hipex helps solve these problems. Hipex is used to extract layout netlist, parameters, and parasitic devices from an IC design with deep-submicron process technology. Hipex contains the following parts that perform fast and accurate netlist and parasitic extraction for full chip design:

- NET – for hierarchical netlist extraction
- C – for parasitic capacitance extraction
- R – for parasitic resistance extraction
- Netlister – for RC distribution and netlists output

Hipex tool is under permanent development: new features are added, current algorithms are updated and improved. One new global Hipex improvement is using central Hipex Database that connects tools to each other simplifying parasitic extraction and netlists output. This article describes Hipex improvements including new flow based in this database.

2. New Hipex Flow

New Hipex flow includes several stages that will be described below and are shown in Figure 1.

The hierarchical netlist extractor, Hipex-NET, is basic part of layout extraction process. It uses GDSII or CIF layout file and user-defined technology file as input files that contain all necessary information for netlist extraction. During device parameter extraction, Hipex-NET also performs Electrical Rule Checking (ERC). Once it is done, Hipex-NET outputs the extracted data to Hipex Database (HDB), which is used as input for parasitic extraction and netlisting. HDB contains all information on extracted nets and devices, including geometry.

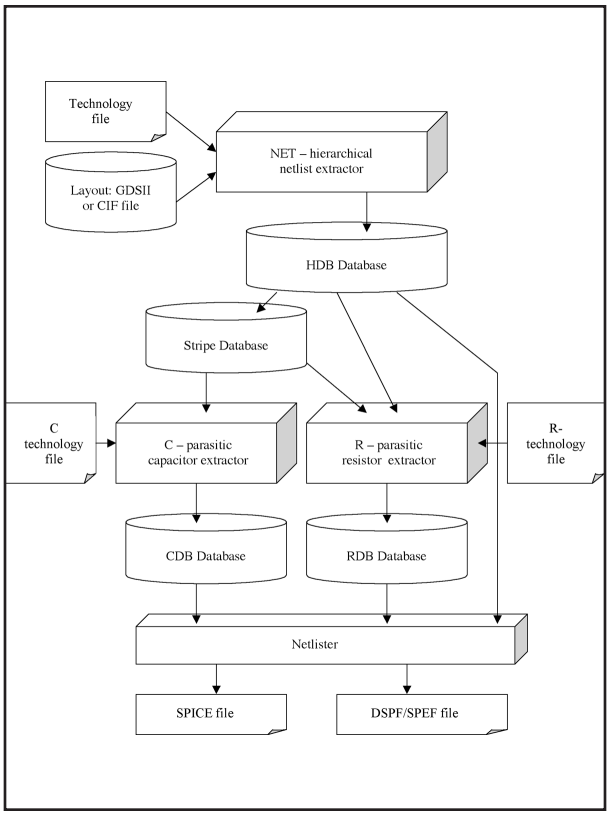

Figure 1. Hipex Flow.

Hipex-NET supports backannotation, i.e., it can use schematic net names to maintain names from the original netlist. Backannotated net and device names obtained by Guardian LVS are used for this purpose and saved in HDB, too. Since these names are saved in HDB they can be used for output of any backannotated netlists.

New Hipex Netlister uses HDB for output extracted netlist in SPICE format in hierarchical or flat forms.

Hipex parasitic extraction uses Stripe Database (SDB), which is generated from HDB. It contains information on nets for which parasitic extraction is to be performed. It can be the all nets (full chip extraction) or selected critical nets (selected net extraction). Saving data in SDB permits to process big layouts because layout is divided into stripes with appropriate size and each stripe is processed separately.

Hipex C performs parasitic capacitance extraction based on data from SDB and user-defined technology file. Technology file contains rules for area, fringe and lateral capacitance. Capacitance coefficients for these rules can be obtained from 3D solvers like EXACT or another third party tools. Hipex C includes basic built-in models for fringe and lateral capacitance, but user can implement his own models for more accurate parasitic extraction using LISA procedures. Hipex C provides a wide set of extracted geometrical parameters for this purpose.

The result of Hipex C execution is Capacitance Database (CDB), which includes parasitic capacitance for selected nets. CDB is incremental database, so data obtained for new selected nets will be added to CDB, and in this case it isn't necessary to run Hipex C twice for the same nets.

Hipex R extracts parasitic resistors for nets that are included in SDB. Technology file for Hipex R contains rules for extraction wire and contact parasitic resistors. The parasitic resistor extraction is performed net by net. Each net is extracted in flat mode. It means that parasitic resistors for net are assigned to top cell where net begins. Hipex R results are stored in incremental Resistance Database (RDB) that contains subnets information and parasitic resistor values.

Hipex Netlister uses data from HDB, CDB, and RDB to produce parasitic netlists in three formats: SPICE, DSPF and SPEF. SPICE netlist can contain parasitic capacitors or resistors only, or both as distributed RC network. Output capacitors can be coupling or grounded. Also, as it was mentioned above, the netlist can be backannotated by names from schematic netlist.

3. New Layer Mapping

Hipex-NET Mapping

Most of layout files are in GDSII format. One disadvantage of this format is that layout layers have only identification integer numbers but no layer names. That's why GDSII tools allows the user to establish correspondence between layer GDS numbers and layer names (layer map). Original Hipex had two stage mapping procedure. On the first stage GDS numbers were mapped to SLF names and than SLF names were mapped to Hipex layer names. Usually it was two different files. Because SLF format isn't used wide, the new one-step mapping scheme has been implemented. The new mapping command has the following syntax:

```
Hipex layer
        /gds_layer=<integer>
        /gds_type=<integer[,integer, …] >
        /geom_layer=<string>
        /text_layer=<string>;
```

This command maps GDS layer with numbers specified in /gds_layer option and types in /gds_type to Hipex layers specified in /geom_layer and /text_layer. Because Hipex works with separated geometrical and text layers, layer in /geom_layer option contains geometrical data and layer in /text_layer contains text data. Options /geom_layer or /text_layer can be omitted, in this case the corresponding data will be not transferred from GDS file to Hipex. The following example shows command using:

```
Hipex layer
        /gds_layer= 9
        /geom_layer="FMET"
        /text_layer="FMET_HPX_TEXT";
```

This command merges geometrical objects form GDS layers with number 9 and all types to Hipex geometrical layer "FMET" and puts text objects to Hipex text layer "FMET_HPX_TEXT".

In command:

```
Hipex layer
        /gds_layer= 31
        /gds_type=1
        /text_layer="Text_31";
```

only texts from GDS layer with number 31 and type 1 will be put to Hipex text layer "Text_31".

Hipex C Mapping

The mapping command for HPEX-C also has been modified to simplify mapping procedure. New syntax for Hipex-NET to Hipex C layer mapping has the following format:

```
        cup layer <string> [/Hipex_layer=
        <string>[,<string>,…];
```

First <string> parameter is Hipex C layer name, and Hipex-NET layer names are specified in /Hipex_layer option. If /Hipex_layer option is omitted, the parameter <string> is the same layer name for both Hipex C and Hipex-NET. It is possible to map several Hipex-NET layers

to one Hipex C layer in one command. All Hipex-NET layers should be listed in /Hipex_layer option. For example, the following command combines two Hipex-NET layers “PSUB” and “NWELL” into one Hipex C layer “SUBS”:

```
cup layer SUBS  /Hipex_layer= PSUB,NWELL;
```

4. Improved Parasitic Extraction

New improvements and modifications have been done for parasitic extraction part too.

Hipex C

New commands provide effective means for modeling vertical shielding and charge sharing effects.

Hipex C produces CDB, which contains all information on parasitic capacitors. Hipex Netlister uses this database to output parasitic capacitors to SPICE, DSPF or SPEF files.

Hipex R

The syntax of new Hipex R commands also has been simplified. As in the previous version of Hipex R there are two kinds of commands. First command defines wire parasitic resistor and second one defines contact parasitic resistor. The improvement is that parasitic resistor body and terminal layers obtain autogenerated names. The new parasitic commands have the following syntax:

```
rpx define_parasitic wire
     /layer=<string>
     /contact_cluster = <double>
     /contact_oversize = <double>
     /pres_sheet_resistivity_value=<double>;


rpx define_parasitic contact
     /layer=<string>
     /top=<string>
     /bottom=<string>
     /pres_area_resistivity_value = <double>;
```

Because one contact layer can connect different pairs of layers, the parasitic contact command contains two additional parameters that define connected layers. It is top and bottom parameters in this command.

Hipex R works with flatten nets, that simplifies internal algorithm, increases accuracy and speeds up parasitic extraction procedure. Hipex R results are saved in RDB, which is incremental database.

RDB contains all subnet information and parasitic resistors values. Netlister uses RDB to output parasitic resistors to netlists.

5. Hipex Netlister

New part of Hipex flow is Netlister. Hipex Netlister performs all netlists output, including SPICE, DSPF and SPEF files. It uses data from HDB, CDB, and RDB. Therefore, netlists can be output it any time if HDB, CDB, and RDB are available.

For parasitic netlists, Netlister performes RC distribution if both CDB and RDB are present.

There are two Netlister commands that output netlist in SPICE or DSPF/SPEF formats.

The command for SPICE output has the following format:

```
netlist spice
        [/hier | /flat]
        [/norc | /c | /r | /rc | /rcc [/nets=...]]
        [/noba | /ba]
        <file_name>;
```

default options are /hier, /norc, /noba.

Options /hier and /flat define hierarchical or flat netlist output.

Option /norc suppress output of parasitic elements.

Options /c,/r,/rc,/rcc,/nets=... define parasitic element output. Parasitic capacitance can be output if CDB is present, and, correspondingly, parasitic resistors can be outputted if RDB is present.

Option /c defines parasitic capacitors output only.

Option /r defines parasitic resistors output only.

Option /rc defines distributed RC network with grounded capacitors output.

Option /rcc defines distributed RC network with coupling capacitors output,

Option /nets= defines list of parasitic nets for which coupling capacitors will be output. Capacitors for other parasitic nets will be grounded. If this option is omitted coupling capacitors will be output for all parasitic nets.

Options /noba or /ba define backannotation mode of netlist output.

DSPF and SPEF files are output by command:

```
netlist parasitic
        [/file_path=<directory_name>]
        [/dspf | /spef]
        [/cc [/nets=...]]
        [/noba | ba]
        [/cell=<cell_name>]
```

Option /file_path defines path to output DSPF or SPEF file.

Options /dspf and /spef define file format.

Option /cc defines coupling capacitor mode for nets that listed in /nets option.

If /nets option is omitted, all capacitors will be considered as coupling.

Options /noba or /ba define backannotation mode of netlist output.

Option /cell defines the cell name, which will be considered as top cell. Default value of top cell is taken from HDB. Output file name has fixed name <top_cell_name>.dspf or <top_cell_name>.spef.

6. Conclusion

Recent Hipex improvements make it more powerful and flexible. New Hipex execution flow simplifies its using and gives user new possibilities to make more accurate and fast parasitic extraction.