Managing Circuit Simulation Using VWF

Introduction

VWF, Virtual Wafer Fab, is a software tool used for performing Design of Experiments (DOE) and Optimization Experiments. Split-lots can be used in various pre-defined analysis methods. Split parameters can be defined for any process, device and circuit simulators in VWF. In addition, all simulation queues can be managed and the simulation results are displayed in a worksheet in VWF.

VWF can define values of split parameters or review all results of circuit simulation.

Preparation for Simulation Circuits

A simple comparator circuit is prepared for running SPICE simulation using the Gateway Schematic Editor. See Figure 1.

In this case, 3 split parameters are defined using .PARAM in Gateway. See Figure 2.

- • Power Voltage : "VDD"
- • Temperature : "tempval"
- • Output load capacitor : "capval"

This is not only a SPICE model library and analysis statements, but also a measure statement in the control card.

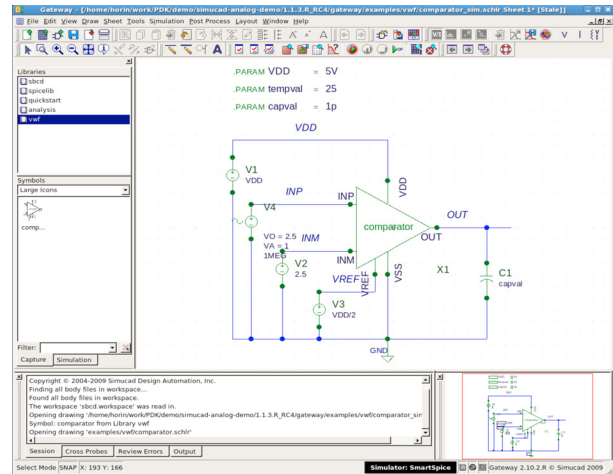Figure 1. Comparator circuit.

Figure 2. PARAM setups in a simulation top circuit.

See Figure 3. The following measure calculations are performed to monitor the rise/fall delay times for an output signal "OUT" when 2 input signals "INP" and "INM" are crossed. They are specified within 25n seconds for convenience.
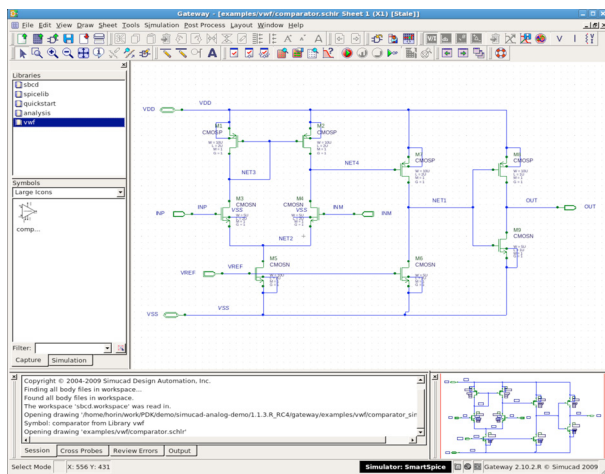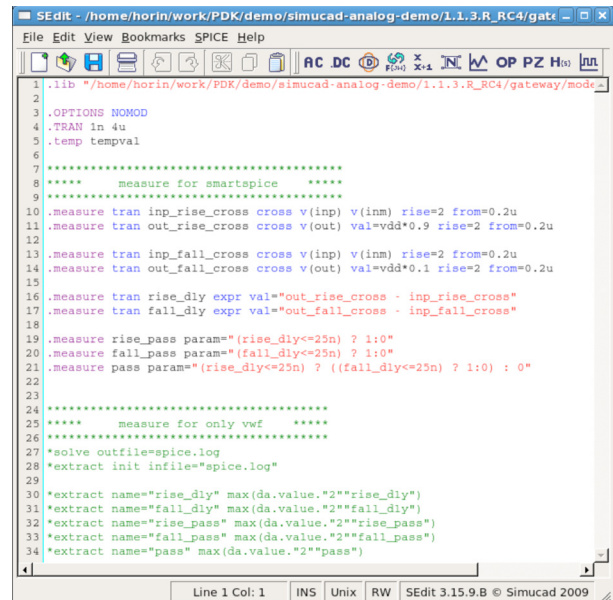

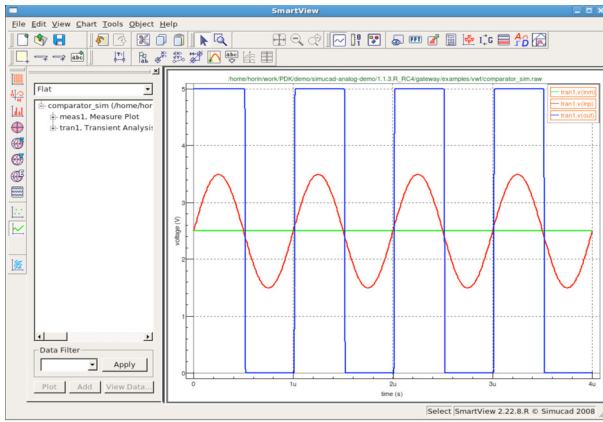Figure 3. measure statements in the control card.

Figure 4. Simulation result with a center condition.

- rise_dly: delay time when output signal rise
- fall_dly: delay time when output signal fall
- rise_pass: If rise_dly is within 25ns, "1". Else, "0".
- fall_pass: If fall_dly is within 25ns, "1". Else, "0".
- pass: If rise_pass, fall_pass are both within25ns, "1". Else, "0".

A section with comment delimiters from the 24th line is used only in VWF for displaying a list of measurement results.

A simulation with center condition is run in advance using SmartSpice.

A simulation result can be displayed as a transition of output "OUT" when an input sine wave "INP" crosses an input dc voltage "INM". See Figure 4

Running SPICE Simulations for 27 Conditions and Review the Results Using VWF

3 parameters, "VDD", "tempval" and "capval" are split each with 3 conditions, this creates a total of 27 conditions, for VWF. Circuit designers use the ".alter" statement mainly for split simulations, but sometimes a lot of simulation setups are laborious for designers.
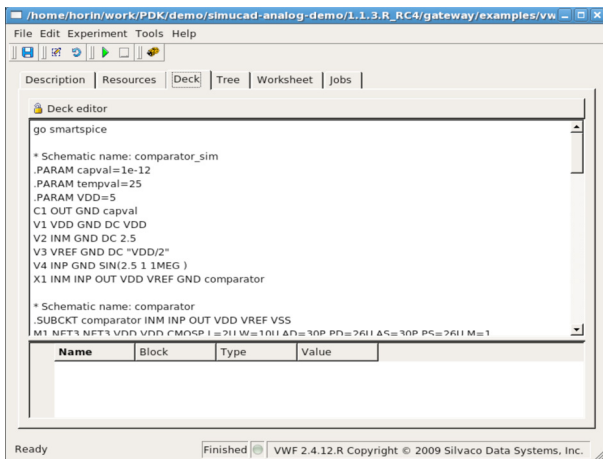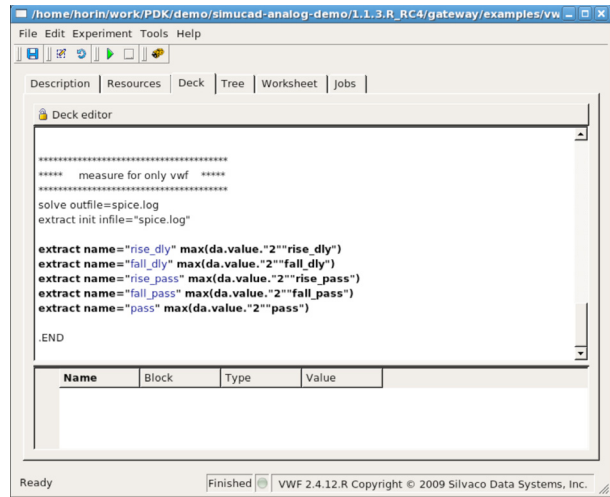

Figure 6. Edited bottom section.

VWF helps designers to set up split conditions, monitor simulation status, and review all simulation results.

First, launch VWF in file mode. (You can select firebird database mode, if necessary.)

%vwf –filemode &

Import the edited input deck form generated one by Gateway.

1. Remove a section with comment delimiters of header and insert "go smartspice" . See Figure 5

2. Remove comment delimiters of bottom to display a list of simulation result in VWF. See Figure6

After loading the edited input deck, define 3 split parameters, "capval", "tempval" and "VDD" in the "Deck editor" tab. See Figure 7.

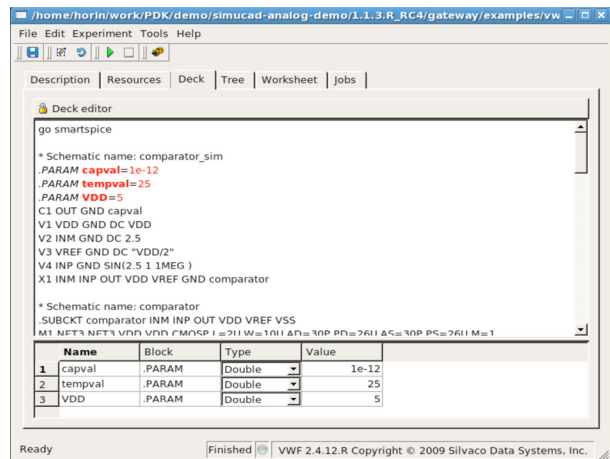
Figure 5. edited header section.
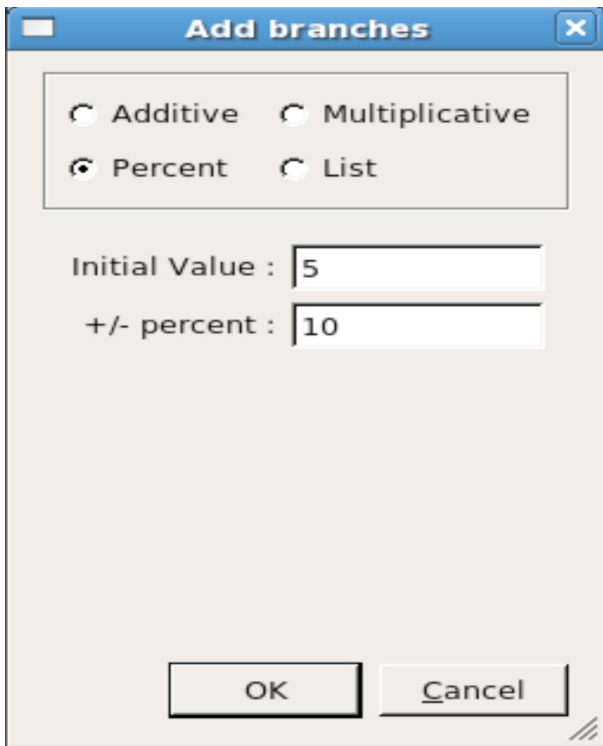

Figure 7. Definition of split parameters.
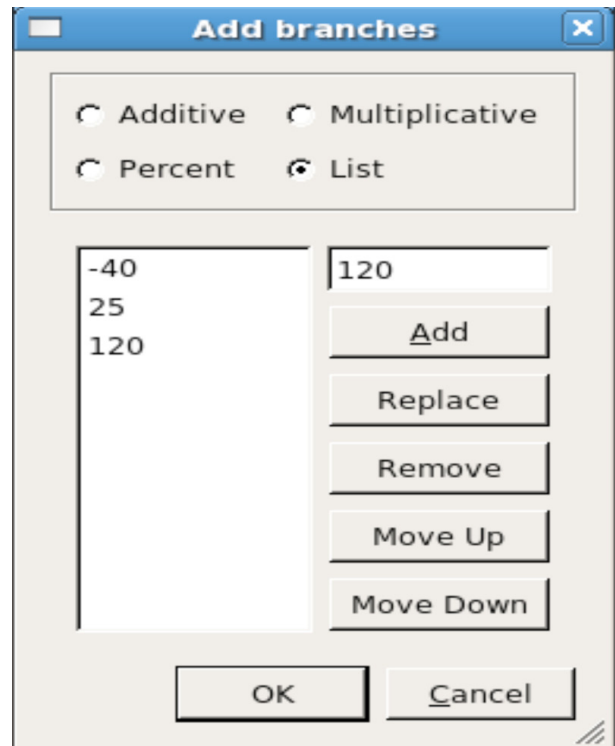
Figure 8. split VDD.

Figure 10. Split tempval.

After definition of these split parameters, you can set 27 conditions automatically in only 3 steps in "Tree" tab.

1. split "VDD" value in 5V±10%. See Figure 8,9.

2. split "tempval" value in -40,25,120. See Figure10,11

3. split "capval" value increased 1e-12 from default. See Figure12,13

After that, it is able to queue all or arbitrary conditions to run the simulation. VWF supports SUN Grid Engine for run simulations.

"Fragment status" in the "Tree" tab shows simulation status of each queue. See Figure14
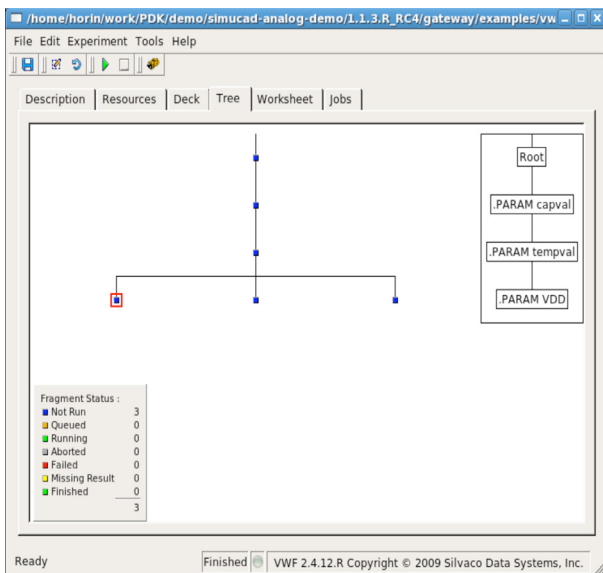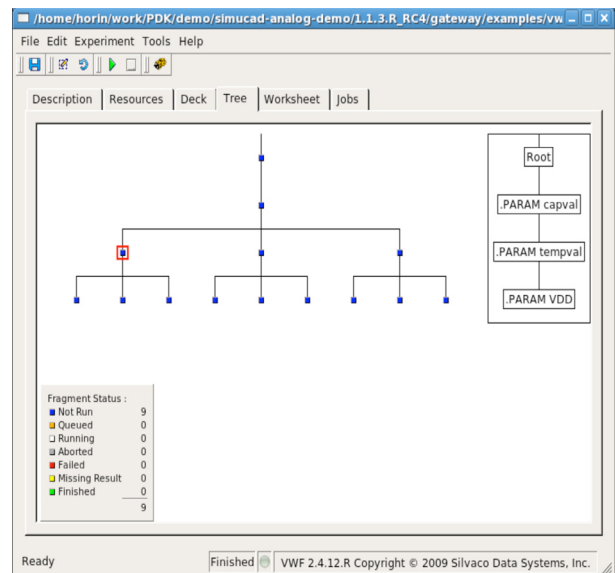

Figure 9. Three conditions tree after split VDD.
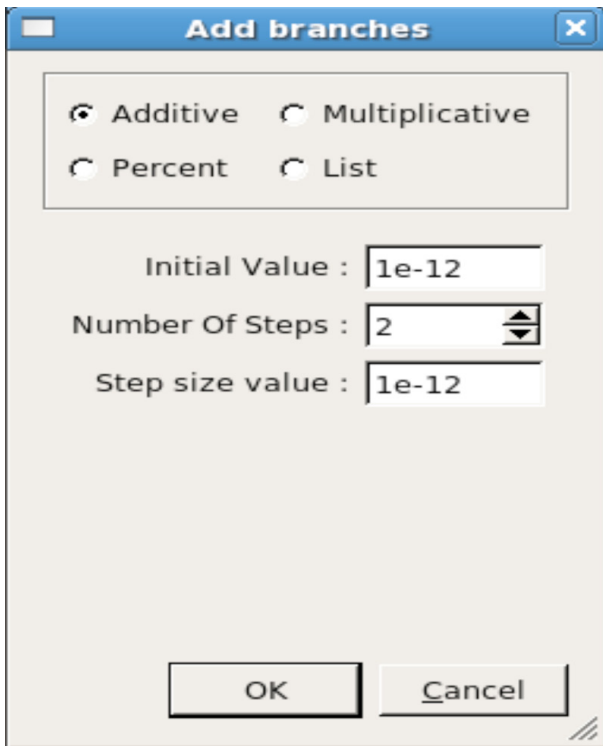

Figure 11. Nine conditions tree after split tempval.

Figure 12. Split capval.

A list of all simulation results in the "Worksheet" tab after running simulations makes it very easy to review which conditions are pass or fail because all simulation conditions and results are in the lists. See Figure 15. In these results, it is easy to find that increased load cap, high temperature and lower power condition is severe for the specification.
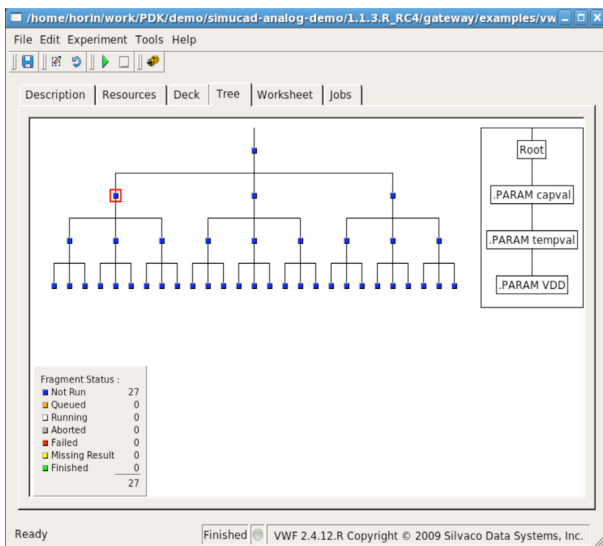

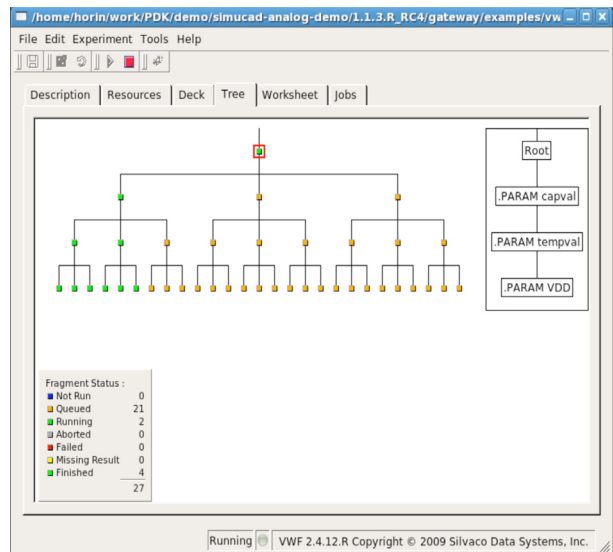Figure 13. Twenty-seven conditions tree after split capval.
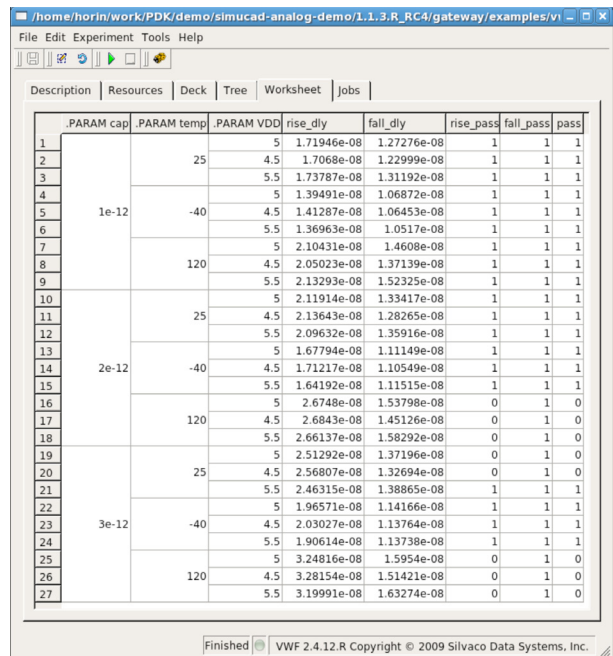

Figure 14. Simulation status in "Tree" tab.

Figure 15. A list of simulation results.

Conclusion

VWF is a good management tool for circuit simulations because it is very useful to split a lot of conditions automatically and review the simulation results quickly. VWF provides a strong simulation environment for not only process and device simulation, but also analog circuit simulation with a lot of conditions.