Debugging Verilog-A Flow Under Windows

Because the Windows platform does not have a native C compiler it is necessary to install a separate C compiler program that is not shipped with the Silvaco software. For initial guidance refer to SmartSpice User's Manual Volume 2, Chapter 10.

If a C compiler has been installed and the path setup correctly then this flow below may be used to trace the problem.

If a Verilog-A module does not work in a SmartSpice simulation, then, use the following steps to find the problem in the Verilog-A flow.

A. See if you can generate a C file.

1. In a DOS window set the Current Working Directory (CWD) to the folder where you have the <file_name>.va
2. Example: **D:\colins\Smartspice\test_decks\VLGA_diode**
3. Run command <full_path1>/veriloga.exe <file_name>.va -l
4. Example: V**:\lib\smartspice\3.11.47.C\x86-nt\VLGA\veriloga.exe diode.va -l**
5. This will produce a folder: "SilvacoVLG" in the CWD area.
6. This folder will contain (for example):
   - **SilvacoVLG\1.6.47.R\x86-nt\diode.log**
   - **SilvacoVLG\1.6.47.R\x86-nt\diode.va_err**
   - **SilvacoVLG\1.6.47.R\x86-nt\map.vlga**
   - **SilvacoVLG\1.6.47.R\x86-nt\photodiode_10988.c**

   Check for example file: **SilvacoVLG\1.6.47.R\x86-nt\diode.log**

   Errors: 0 Warnings : 0

If there are errors or warnings then these need to be fixed before proceeding to the next step.

The description of the error can be found in the **SilvacoVLG\1.6.47.R\x86-nt\diode.va_err** file.

B. Produce .dll file used in SmartSpice simulation run

1. Run command <full_path1>/veriloga.exe <file_name>.va -l -vcc -libvlgpath <full_path2>

   Example: **V:\lib\smartspice\3.11.47.C\x86-nt\VLGA\veriloga.exe diode.va -l -vcc -libvlgpath V:\lib\modellib\1.6.0.R\x86-nt**

   Check that the following files were produced:

   - **SilvacoVLG\1.6.47.R\x86-nt\diode.log**
   - **SilvacoVLG\1.6.47.R\x86-nt\diode.va_err**
   - **SilvacoVLG\1.6.47.R\x86-nt\map.vlga**
   - **SilvacoVLG\1.6.47.R\x86-nt\photodiode_13225.dll**

If you generate this unique .dll file name then you can try to run the input deck in SmartSpice

C. Run example Input deck in SmartSpice

1. Run an input deck that contains a reference to a Verilog-A module

   Example: **diode.in**

   If there are errors then SmartSpice will indicate what the problem is.

NOTE:

<full_path1> full path to veriloga.exe

<full_path2> full path to libVLG_version_number_R.lib file (e.g. libVLG_1_6_63_R.lib)