Importing Standard Design Libraries Using EDIF 2 0 0

This Simulation Standard addresses the importing of EDIF 2 0 0 schematics designed with default vendor design libraries. The process of editing an imported schematic of this type begins with recognizing the symbols that are instantiated on the imported drawing by the EDIF imported schematic. Many of the analoglib and basic library primitive symbols have a similar representation in a default Gateway library. The spicelib is the primitive library Gateway uses for all active and passive spice type symbols. Other special symbols such as ground pins, schematic input/output pins, and power symbols are included in this library. The goal is to find as many symbols on the imported drawing that can be changed to Silvaco symbols with minimum redrawing and editing.

Export from Vendor

Figure 1 illustrates an example schematic for this procedure. The schematic is named 'current_mirror' and was saved into a library named 'test'. This schematic was captured using symbol and SmartSpice views from the Virtuoso analoglib library. Export the schematic in EDIF 2 0 0 format from the Cadence environment into a file with a *.eds or *.edn extension for *Gateway* to import.

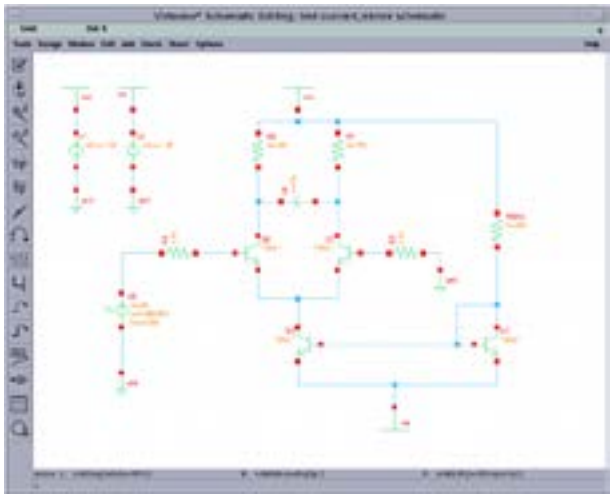

Figure 1. Schematic captured in Virtuoso®.

Import into Gateway

When the EDIF file is ready, it may be loaded into *Gateway*.

1. Load a workspace into *Gateway* with at least one library. In this example, a workspace with only a spicelib library is loaded
2. Click File->Import->EDIF… and select the file and check appropriate boxes as shown in Figure 2
3. Click OK

As the file is imported and converted, the libraries being imported will be written and added to the workspace. In this example, the 'spicelib' was the original library in the workspace before conversion. After conversion, the 'analoglib' and 'test' libraries were added. Also, during conversion the session window scrolls as each instance of every drawing is processed and cells are written into the libraries. This is a partial report of the conversion. At the end of it, a message is written such as:

Processing library 'test' (EDIF level 0)

Processing cell 'current_mirror'

WARNING: Signal name 'GND!' has been converted to 'GND'

WARNING: Signal name 'VSS!' has been converted to 'VSS'

WARNING: Signal name 'VCC!' has been converted to 'VCC'

Phase 3 complete

EDIF import completed successfully

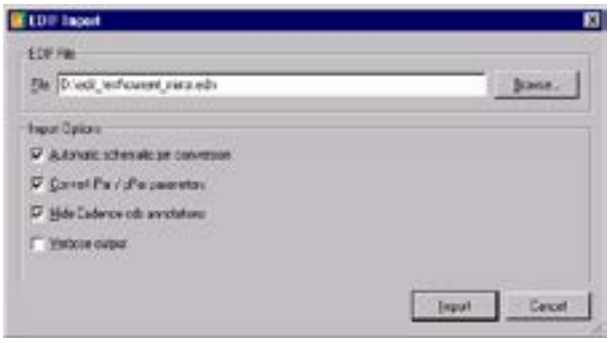

Figure 2. Set Import settings

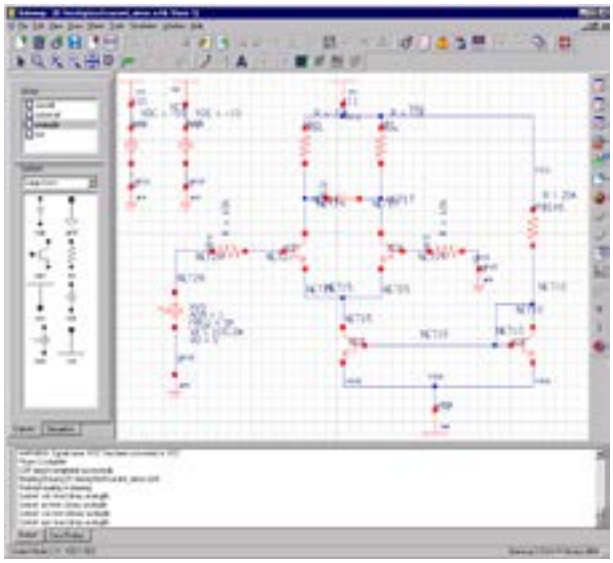

Figure 3. Imported Schematic in Gateway.

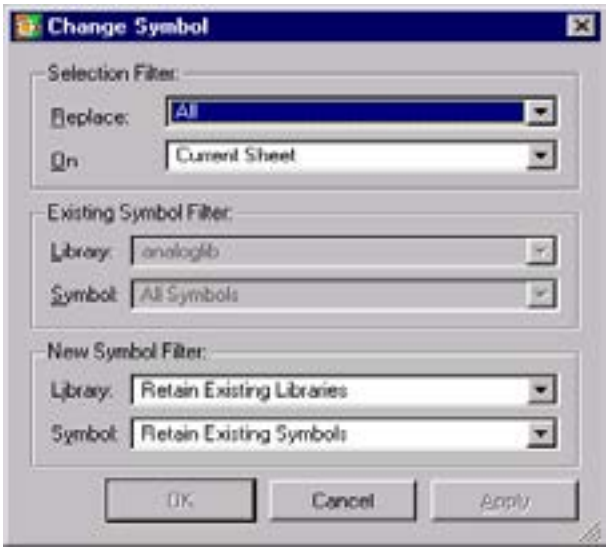

Figure 4. The Change Symbol Dialog,

At this stage, the imported schematic may be opened for edit. Open the file named 'current_mirror.schlr' in the .\ TEST directory. When the schematic opens, click on the 'analoglib' in the library pane. The symbols written into the 'analoglib' library during the EDIF in process show in the symbol pane below. Figure 3 displays the schematic opened in Gateway after importing it.

At this point, the EDIF conversion has done its job and created the cellviews as they existed in the original schematic capture environment. Most of the time, these schematics must be edited to generate a useful netlist that SmartSpice can understand. To do this, some basic steps must be followed. Most symbols should be wired as they were in the original Virtuoso drawing such that moving the symbols will rubberband the wires to the symbol pins. The basic steps for editing are as follows:

1. Use the Change Symbol dialog to update the schematic with spicelib symbols (that have *SmartSpice* attributes for netlisting). This replaces instances from 'analoglib' with 'spicelib' instances. Goto Tools-> Change Symbol and see in Figure 4
2. Set the New Library to '*spicelib'* as seen in Figure 5
3. Press OK
4. Select Edit->Select All
5. Select Edit->Align Attributes – the drawing should look like Figure 6
6. Now perform a check drawing – the error dialog shows in Figure 7
7. Note the four errors are the same and are due to mandatory attributes that have not been assigned a value. The reason is that some symbol attribute names are not the same from vendor to vendor. Here is a case of simulator attributes (MODEL in Spectre®) and (MNAME in *SmartSpice*) being different and need to be changed

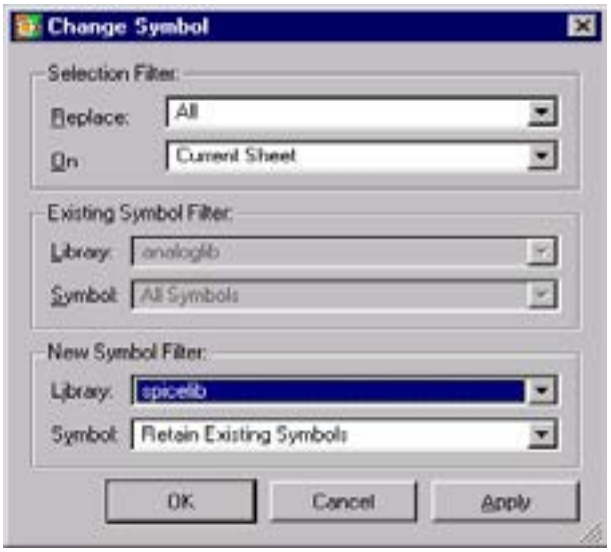

Figure 5. Changing the library origin of the instances.

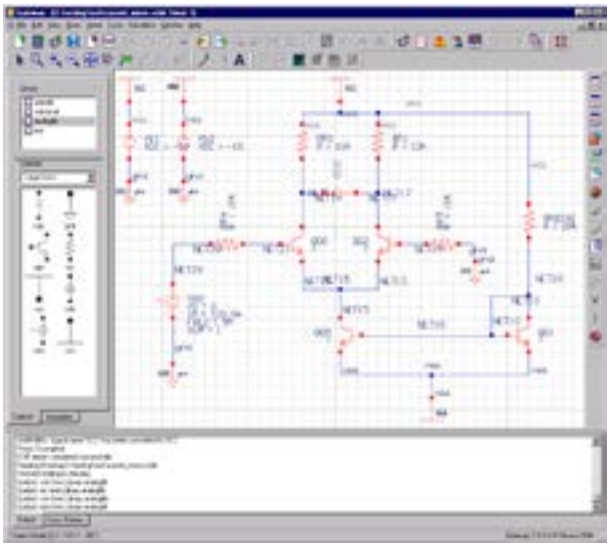

Figure 6. Schematic after Change Symbol is performed.

8. Make the changes by double clicking theQQ0 BJT instance – then see the dialog in Figure 8 and make the dialog look like Figure 8

9. Click OK

10. Create and View the netlist – see Figure 9

The schematic may be further edited for aesthetic purposes to include aligning attributes, changing the visible display for certain attributes, and turning net names on/off. See the *Gateway.pdf* manual for full list of editing features.

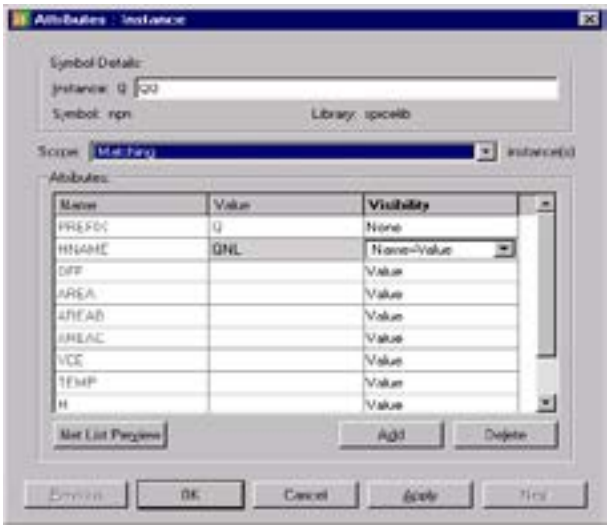

Figure 8. Symbol Attributes Dialog.

Figure 7. Review Errors Dialog.

Conclusion

Interchanging graphical data for schematics is not as clearly defined as it is for layouts. EDIF is limited in capability as compared to foudnry-driven formats like GDSII. Because of this, each CAD vendor is responsible for making the EDIF import/export features in their software as useful and productive as possible. Because schematics captures between vendors vary greatly, most of the time additional work is required after EDIF import to produce a netlist that is ready to simulate.

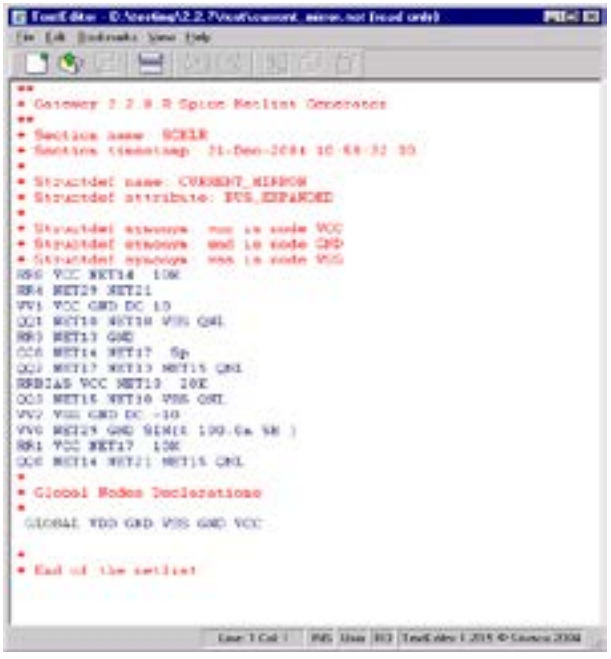

Figure 9. SPICE netlist generated from ***Gateway***.