Schematic Driven Process Corners Analysis

Introduction

This application note illustrates how process corner simulation is run from the schematic design in Gateway. The subject is a five stage current-starved VCO that is captured in the Gateway Schematic Editor. After a SPICE netlist is generated from the schematic, a simulation profile is built using a 1.8V 0.18um UMC process. A transient analysis will be set up that will plot the input voltage and output voltage change over time. SmartSpice will then run the first transient analysis, and then switch to a second and third process corner to complete the simulation. This design uses 22 Berkeley Bsim3v3-type transistors and one resistor.

Capturing and Netlisting

Figure 1 shows the instance attribute for one of the PMOS devices. All instance attribute data is entered in these dialogs for the n-type and p-type devices. As seen in Figure 1, the MNAME field is set to P. MNAME is the SmartSpice attribute for the model name to be used for the instance. Since the model file uses P for the p-type devices, the instances must be set to match on the schematic. The MNAME field, then, is used to link instances of devices to their SPICE models. The model used for the n-type devices is N, so all nmos devices on the schematic will show that for the MNAME field.

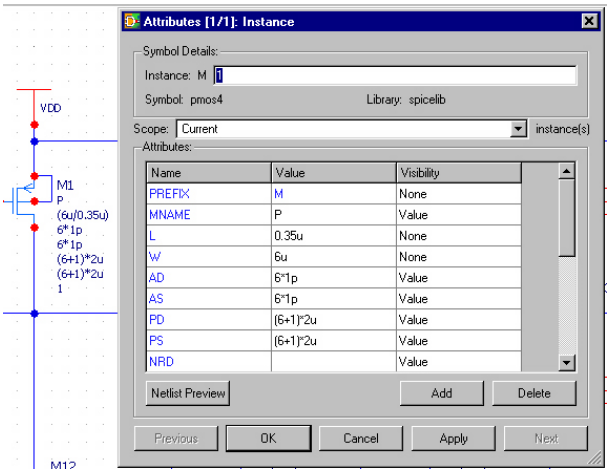

Figure 1. Instance attributes dialog.

Figure 2 shows the completed VCO schematic. The next step is to check the drawing for errors and then to save it. once it is determined that the schematic is clean, a SPICE netlist is generated by Gateway. Figure 3 shows a portion of this .net file. This netlist file is the first of three parts of the input deck file that actually run in SmartSpice. The next two parts of the input deck are discussed in the next section.

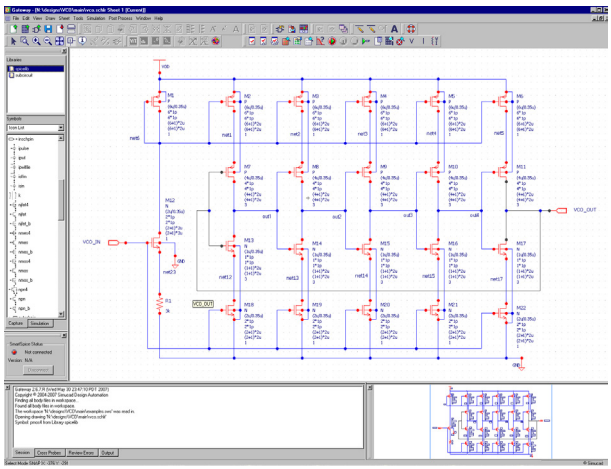
Figure 2. VCO schematic.

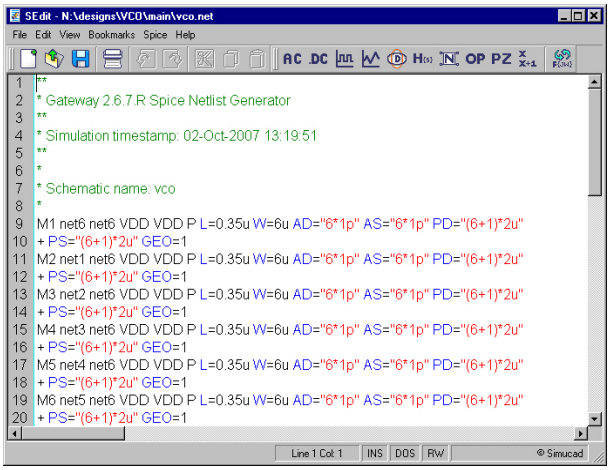

Figure 3. SPICE netlist.

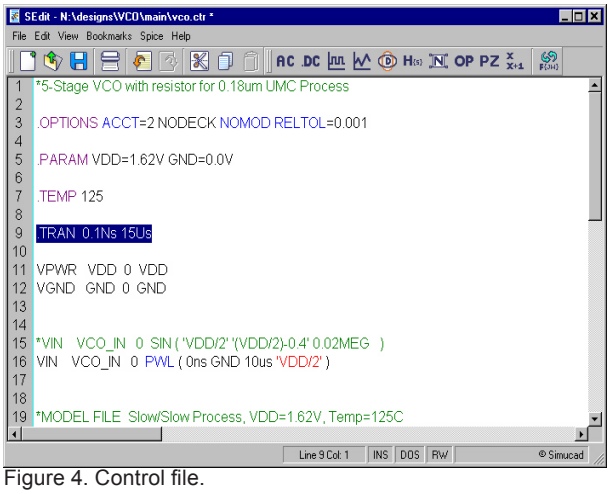

Figure 4. Control file.

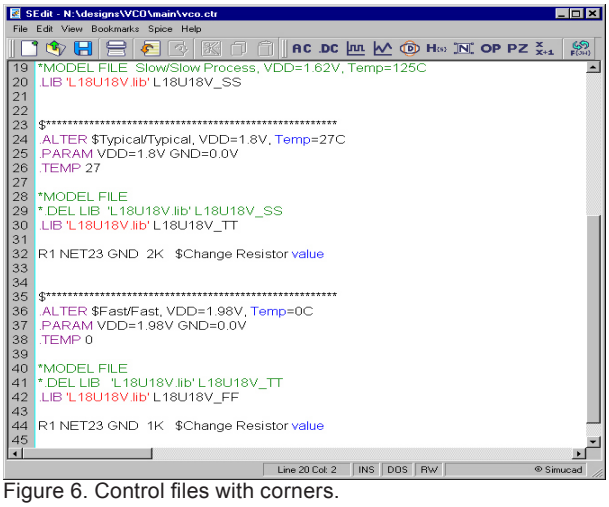

Figure 6. Control files with corners.

Pre-Simulation

After a netlist is generated, the next step is to build a simulation profile. The two remaining parts of the input deck file are the control file and the cross probe statements. The control file contains all SPICE instructions on what to run and how to run the simulation. The cross probe file contains the statements for saving and plotting data.

The control file (Figure 4) is used to specify that the duration of the transient analysis is 15us. Also this is where SPICE options are added and sources may be defined if they are not drawn on the schematic. In this case, a PWL input is defined for the circuit. At this point the model information is ready to be added. Since corners will be run, the library file format is easiest to use. Using the .LIB statement to choose the UMC file, the first corner is selected to run. In this case, the SS or Slow/Slow case is selected first. Figure 5 shows the dialog for choosing the library file and then the corner library within.

Now the control file has a .LIB statement to link SPICE models for this process corner. Next, the .ALTER statement is used to effectively rerun the simulation again for everything between the .ALTER and the .END statement, or to the beginning of the next .ALTER. This is how you can change elements in the matrix and parameter data, as well as changing from one process corner to the next.

Then the second (Typical\Typical) and third (Fast\Fast) corners are added for simulation. Parameter values may be changed from run to run also, as shown in Figure 6.

Finally, Gateway is set to Simulation mode, and the input and output nodes of the VCO are selected to be plotted in real-time as the simulation progresses. While the simulation runs the output waveforms are displayed in real-time as shown in Figure 7.

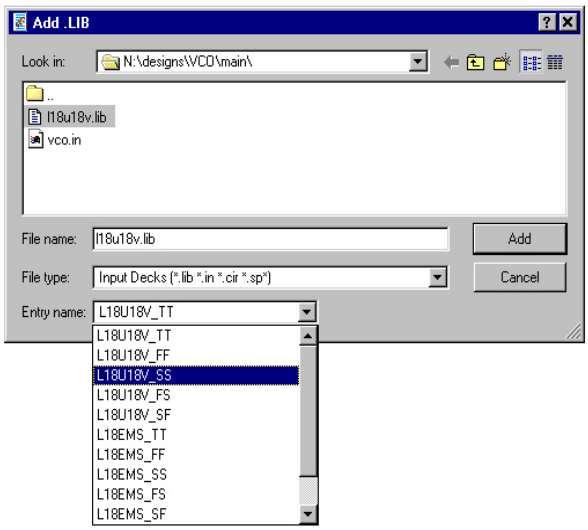

Figure 5. SPICE library and corner dialog.

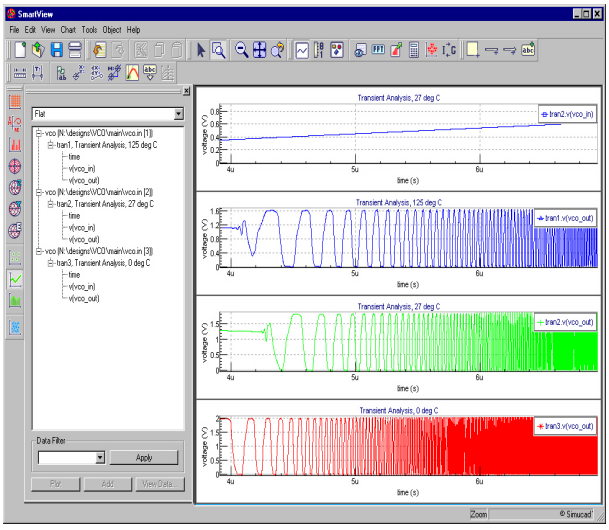

Figure 7. Resulting waveforms.